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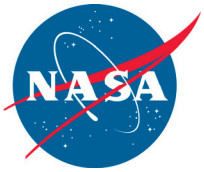

Reliability of Area Array Packages with 1500–2500 I/Os

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NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

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Objectives and Products

Commercial-off-the-shelf ball/column grid array packaging (COTS BGA/CGA) technologies in high reliability versions are now being considered for use in a number of National Aeronautics and Space Administration (NASA) electronic systems. Understanding the process and quality assurance (QA) indicators for reliability are important for low-risk insertion of these advanced electronic packages. This report summarizes the extremely limited reliability information on 1500 to 2500 input/output (I/O) flip-chip ball-grid-array (FCBGA) technologies in comparison to a more widely available reliability data for their counterpart plastic BGAs (PBGAs) with lower than 1000 I/Os. FCBGA packages are generally offered for the advanced high-performance field gate programmer array (FPGA) integrated circuit (IC) microelectronic systems. Unlike conventional packaging in which the die is attached to the substrate face up and connection is made by using wire, the solder bumped die in FCBGA is flipped over, hence the term “flip chip,” and provides connection.

This report presents test data for FCBGA packages with 1704 I/Os and 1-mm pitch. It presents manufacturing yield and quality assurance results for test vehicles assembled with FBGA1704, fine pitch BGA (FPBGA) with 432 I/Os and 0.4-mm pitch, and PBGA with 676 I/Os and 1.0-mm pitch packages. These BGA packages were assembled onto printed circuit/wiring board (PCB/PWB) using standard tin-lead solder alloy approved for NASA applications. Assembly yield provided manufacturing challenges associated with assembly of a large FCBGA1704 enveloped with FPGA432 packages. FCBGA1704 packages were assembled using either a vapor-phase reflow machine or a rework station. Assembly integrity was evaluated by monitoring daisy chain values and performing x-ray characterization. Then they were subjected to thermal cycling and dynamic loading via repeated control drops. This report also presents environmental test results and failure characterizations before and after FCBGA1704 sample x-section using x-ray and various features of scanning electron microscopy (SEM). Finally, the report provides QA indicators and qualification guidelines generated based on the test results for the FCBGA1704, PBGA676, and FPBGA432 packages and assemblies. The qualification guidelines based on the test results will facilitate NASA projects to use very dense and newly available packages with the known risk on reliably and mitigation, allowing more processing power in a smaller board footprint and lower system weight.

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1. Organization and Topics of Report

This report first provides a literature survey for designing, manufacturing, and reliability test results for area array packages with 1500 to 2500 inputs/outputs (I/Os). It then presents test matrix on design, yield, and workmanship defects on assembly and environmental testing, including thermal cycle and mechanical drop-test evaluation results for FCBGA1704, FPBGA432, and PBGA676 I/Os packages assembled onto printed circuit/wiring boards (PCBs/PWBs). Finally, it summarizes lessons learned from test results for assembly and environmental testing along with optical, scanning electron microscopy (SEM), and x-ray photomicrographs showing damage progress. Topics discussed in this report are as follows:

- Executive summary providing key background information, test results, and lessons learned.
- Summary of key parameters that affect assembly reliability of PBGAs and flip-chip BGA (FCBGA) with tin-lead solder based on a comprehensive literature search.
- Comprehensive introductory background on area array package technology, including FCBGA technology, that has been more recently introduced to answer the demand for higher I/O and signal integrity.
- Key advantages of field programmable gate array (FPGA) using FCBGA/BGA technology. Advantages and disadvantages of area array technology are briefly presented.
- Quality assurance documentation of manufacturing processes, including solder paste volumes and photomicrographs of paste print deposition. This report also includes representative processing data for FCBGA1704, PBGA676, and FPBGA432.
- Quality assurance documentation of solder joint assembly using tin-lead solder paste and reflowed with a vapor-phase reflow machine or rework station. Assurance performed through daisy chain continuity test and x-ray characterization.
- Photomicrographs of representative x-ray evaluation showing opens and potential shorts.
- Quality assurance indicators through x-ray characterization of thermally cycled assemblies and establishment if x-rays can detect damage due to thermal cycling.
- Reliability and quality assurance documentation of solder joint damage progress by daisy chain monitoring at intervals due to thermal cycling. Thermal cycles were in the range of –55° to +100°C, –55° to +125°C, and –125°/+125°C. Thermal shock cycle was in the range of –55° to +100°C.
- Results of x-ray characterization of thermally cycled assemblies that was performed to determine quality assurance indicators and to establish if x-rays can detect damage due to thermal cycling.
- Results of scanning electron microscopy (SEM) evaluation of thermally cycled assemblies performed at higher magnifications with a better resolution than optical microscopy. SEM evaluation was performed only prior to a cross-section test sample for failure analysis.

- SEM photomicrographs of cross-sectioned FCBGA1704 after thermal cycles. Damage in package assembly including solder balls and solder joints at the die and at the board level was established.
- Mapping of elemental distribution in solder balls and at the solder joints using x-ray spectroscopy (EDS) of the SEM tool.
- In collaboration activity with Rochester Institute of Technology (RIT) university, report reliability test results, including thermal shock cycle and drops to failure data for FCBGA1704 and other package assemblies. Also report a summary from comprehensive evaluation of PBGA676 and other area array packages with various solder balls, processing conditions, and undefilling.
- In Section 7 Conclusions, a summary of the key findings for FCBGA1704 and other package assemblies are presented.
- In Section 8 NASA Application, specific overall recommendations are provided for NASA and industry to facilitate understanding risks associated with insertion of FCBGA technology for high reliability electronic systems.

2. Executive Summary

This report presents reliability and thermal cycle test results for test vehicles (TVs) built with daisy-chain, non-functional area array plastic packages (see Figure 1) with up to 1704 inputs/outputs (I/Os). The biggest package was flip-chip ball grid array (FCBGA) and 1.0-mm pitch, representing one of the largest commercial-off-the-shelf (COTS) area array packages available in daisy-chain configuration for reliability evaluation. The other two array package types were plastic ball grid array (PBGAs) either with 676 I/Os and 1.0-mm pitch or with 432 I/Os and 0.4-mm pitch. The FCBA and PBGA packages were assembled onto printed wiring/circuit boards (PWB/PCB) using surface mount processes. Assembly processes were carried out using a vapor phase machine and a rework station to reflow $Sn_{63}Pb_{37}$ tin-lead eutectic solder paste with RMA flux commonly used for high-reliability applications. Packages, however, had conventional tin-lead solder balls specifically offered for high-reliability applications or lead-free solder balls offered generally for commercial applications.

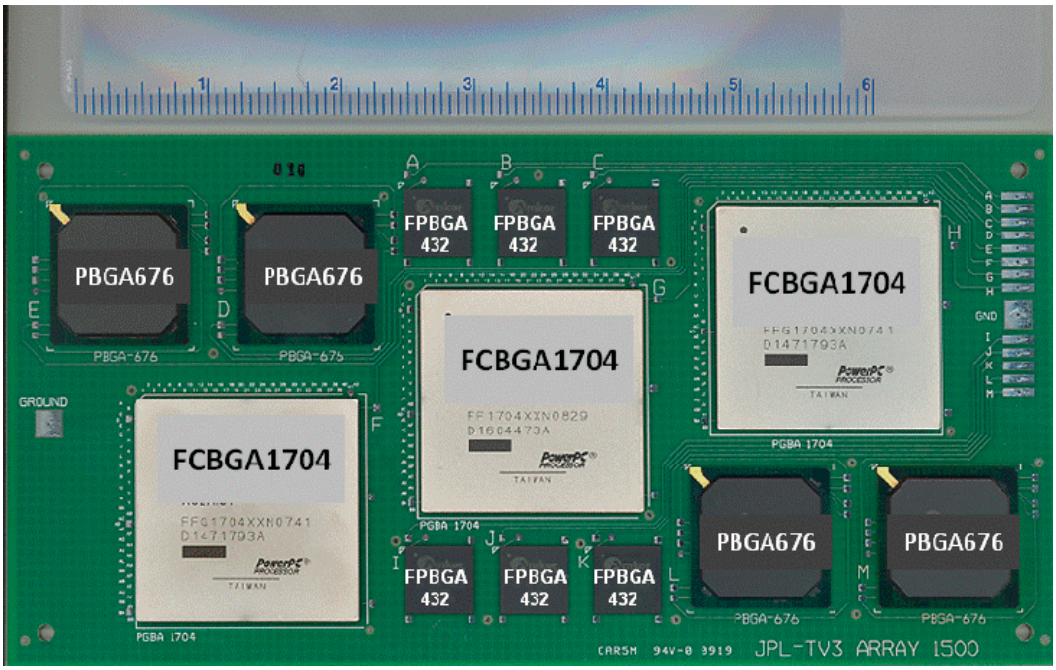

Figure 1. Photomicrograph of a test vehicle with three FCBGA1704 with 1.0-mm pitch, four PBGA676 with 1.0-mm pitch, and six FPBGA432 with 0.4-mm pitch.

BGAs with 1.27-mm down to 0.8-mm pitch (distance between adjacent ball centers) are the only choice for packages with higher than 300 I/O counts, replacing leaded packages such as the quad flat pack (QFP). These types of packages are also used for lower lead counts due to improved density and better characteristics. In addition to higher density due to size reduction, the area array packages also provide improved electrical and thermal performance, more effective manufacturing (improved manufacturability), and ease of handling compared to the conventional surface mount (SMT) fine-pitch leaded parts.

Fine-pitch BGAs with pitches less than 0.8 mm are further miniaturized versions of BGAs, leaded and leadless packages. These electronic packages have low mass and small chip sizes and are generally used for low I/Os (<100) for memory. They now have the potential even for use in higher (>300) I/Os. However, compared to conventional packages, BGAs and advanced area array packages have some key issues (mainly inspection, individual ball re-workability, and in some cases reliability) with the implementation for high-reliability applications.

The key drawbacks of FCBGA, wire-bond BGA (PBGA), and fine-pitch BGA (FPBGA) packages remain the same: inspection capability for interconnection integrity (cracks) and individual solder ball re-workability. In addition, most array packages fall into the category of electronic COTS packages for high reliability applications and therefore are required to be subjected to additional stringent screening with added cost.

The issues with PBGA COTS packages are essentially the same as other COTS issues, including package die source and material variations from lot to lot, availability of packages with radiation hard die, outgassing for materials, and so on. Acceptability of ball integrity attachment before and after high temperature burn-in commonly performed for high reliability applications as well as ball coplanarity should also be considered. Other related implementation aspects including assembly process and controls, especially for finer-pitch array types, and inspection methodology are also key elements in a successful implementation of the area array technology.

More than 1000 I/O packages commonly used for advanced high-performance field programmer gate array (FPGA) come in FCBGA. FPGAs provide the design engineer with a flexible and immensely powerful programming tool for all high-performance electronic systems.

In this report, thermal cycle solder joint reliability of daisy-chain FCBGA package assembly under four thermal conditions is discussed in detail. The results include the nature and extent of damage by x-ray and cross-sectional photomicrographs using scanning electron microscopy (SEM) and solder elemental mapping by x-ray dispersive (EDS) elemental analysis. The report also provides a summary of reliability test results for FCBGA1704 under drop test performed to determine the effects of pre-thermal cycle condition on subsequent drop tests for assemblies with and without corner staking adhesives. Key findings based on a literature survey and test results are presented in Section 7 Conclusions. Experimental results indicate that FCBGA1704 and PBGA676 with 1.0-mm pitch can survive 200 thermal cycles under four different thermal cycle conditions (–55° to +100°C, –55° to +125°C, and –125°/+125°C, and thermal shock cycle in the range of –55° to +100°C). FCBGA 1704 I/O showed minimum signs of damage after thermal cycling evaluated by cross sectioning and SEM evaluation. Key requirements for implementation of NASA electronics systems are discussed in the Section 8 NASA Application.

3. Background Information

3.1 Packaging Technology Trend

Ball grid arrays (BGAs) and chip scale packages (CSPs) are widely used for many electronic applications, including portable and telecommunication products [1]. BGAs with 1.27-mm pitch and 1000 I/Os or less and having tin-lead solder alloys are implemented for high-reliability applications that generally demand more stringent thermal and mechanical cycling requirements. The I/Os are continuously increasing, and plastic BGAs (PBGAs) packages with 1.0-mm pitch up to about 2000 I/Os are offered by package suppliers. PBGAs were introduced in the late 1980s and implemented with great caution in the early 1990s, further evolving in the mid-1990s to fine-pitch BGAs (FPBGAs, also known as CSPs) having much finer pitches of 0.4 and 0.3 mm.

In general, area arrays come in many different package styles, including the plastic ball grid array (PBGA) with ball composition of eutectic $Sn_{63}Pb_{37}$ alloy or slight variations such as $Sn_{60}Pb_{40}$. The ceramic BGA package uses a higher melting ball ($Pb_{90}Sn_{10}$) with eutectic attachment to the die and board. The column grid array (CGA) or ceramic column grid array (CCGA) is similar to a BGA except that it uses column interconnects instead of balls. The lead-free CCGA uses copper instead of a high melting lead/tin column. The flip-chip BGA (FCBGA) is similar to the BGA, except that internally a flip chip die rather than a wire-bonded die is used. For PBGAs with more than 1000 I/Os, FCBGA is used in order to accommodate even the larger number of I/Os required for the flip-chip die within FCBGA package.

Extensive work has been carried out in understanding technology implementation of area array packages for high reliability applications. The work included process optimization, assembly reliability characterization, and the use of inspection tools, including x-ray and optical microscopy, for quality control and damage detection due to environmental exposures [2–11]. In previous investigations, the 1156 I/O PBGA package was the highest I/O PBGA package evaluated for assembly reliability. FCBGA with 1704 I/Os package assemblies were evaluated in this investigation.

3.2 Purpose of this Report

This report provides both a literature survey and comprehensive process/reliability test results for a test vehicle configuration with FCBGA1704 as well as a summary of various test results performed in collaboration with university and industry partners. First, after an introductory summary of PBGA trends and key advantages/disadvantages, it presents key parameters that affect assembly reliability. The parameters included the effect of package I/O, die size and configuration, pitch, and double-sided configuration.

In addition, numerous test vehicles (TVs) were built to determine issues associated with process and reliability of two extreme type PBGA packages. Packages with extremely high I/Os and packages with fine pitch were assembled side by side in a test vehicle to narrow issues associated with their manufacturing on one board. The package configurations were 1704 I/Os FCPBGA with 1.27-mm pitch and FPBGA 432 I/Os with 0.4-mm pitch. A PBGA with 676 I/Os was used as baseline. Both vapor phase reflow and a rework station were used to reflow $Sn_{63}Pb_{37}$ tin-lead eutectic solder paste. Solder balls have either tin-lead or lead-free

solder alloy composition. Process variations for these types of packages as well their yields after process optimization and implementation are also presented. Furthermore, results for thermal cycle reliability of TVs with daisy chain configuration under four thermal profiles are presented and discussed in detail, including optical, x-ray, and x-sectional SEM photomicrographs showing damage progress. Mechanical shock reliability is evaluated by drop tests using assemblies with a priori thermal cycle condition and high I/O package corners with and without staking. In Section 7 Conclusions, key findings based on the literature survey and test results are presented. Finally, key requirements for implementation of the new area array packaging technologies such as FCBGA for NASA electronics systems are discussed in Section 8 NASA Application.

3.3 Area Array Package Technology

Area array packages, e.g., BGAs (see Figure 2) and CCGAs with 1.27-mm pitch (distance between adjacent ball centers) and finer pitch versions with 1-mm pitch, are the only choice for packages with higher than 300 I/O counts, replacing leaded packages such as the quad flat pack (QFP). Area array packages also provide improved electrical and thermal performance, more effective manufacturing, and ease of handling compared to conventional surface mount (SMT) leaded parts. Finer pitch area array packages (FPBGAs), also known as CSPs, are further miniaturized versions of BGAs or smaller configurations of leaded and leadless packages with pitches generally less than 1.0-mm.

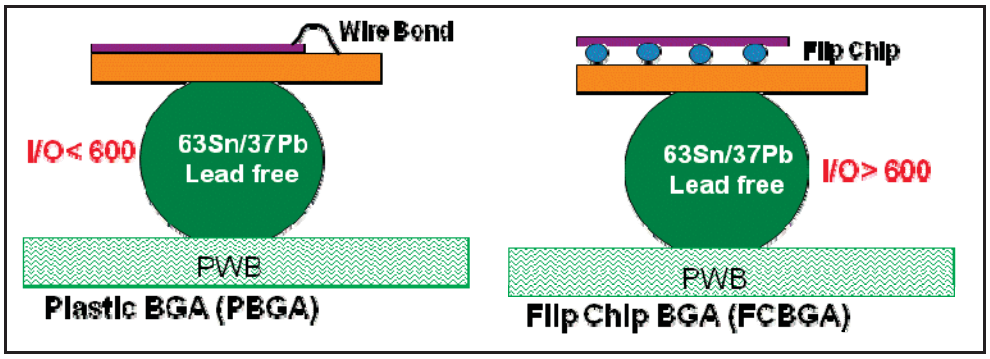

Figure 2. Typical plastic ball grid array with internal wire-bond and flip-chip die for low and high I/O package configurations, respectively.

3.3.1 Advantages of Area Array Packages

Area array packages offer several distinct advantages over fine-pitch surface mount components having gull wing leads, including:

- High I/O capability (Hundreds to approximately 3000 balls can be built and manufactured, but gull-wing leads are limited to less than 300 I/Os.)
- Higher packaging densities (This is achievable since the limit imposed by package periphery for the gull-wing leads is not applicable in the case of area array packages because area rather than periphery is used; hence, it is possible to mount more packages per the same board area.)

- Faster circuitry speeds than gull-wing surface mount components (SMCs) because the terminations are much shorter and therefore less inductive and resistive.
- Better heat dissipation because of more connections with shorter paths.
- Conventional SMT manufacturing and assembly technologies such as stencil printing and package mounting.

Area array packages are also robust in processing. This stems from their higher pitch (typically, 0.8–1.27 mm), better lead rigidity, and self-alignment characteristics during reflow processing. This latter feature, self-alignment during reflow (attachment by heat), is very beneficial and opens the process window considerably.

3.3.2 Disadvantages of Area Arrays

Area array packages are not compatible with multiple solder processing methods, and individual solder joints cannot be inspected and reworked using conventional methods. In ultra-low-volume SMT assembly applications, the ability to inspect the solder joints visually has been a standard inspection requirement and is a key factor for providing confidence in the solder joint reliability. Advanced inspection techniques, including x-ray, need development to provide such confidence for BGA and FPBGAs.

The four chief drawbacks of area array packages are:

- Lack of direct visual inspection capability
- Lack of individual solder joint re-workability
- Interconnect routing between the chip and the PWB requiring a multilayer PWB
- Reduced resistance to thermal cycling due to use of rigid balls/columns

In addition, FCBGA packages that are commonly offered for high-performance field programmable gate array (FPGA) have other drawbacks since they may not be hermetically sealed. During assembly processes, exposure of non-hermetic FCBGA to cleaning solvent/chemicals or excessive moisture could pose serious package reliability concerns. In some cases, it is reported that small vents are deliberately designed between the heatspreader (lid) and the organic substrate to allow for outgassing and moisture evaporation. These vents themselves, however, could become a reliability issue since solvents and other corrosive chemicals could seep through these vents and attack the organic materials and components inside the FCBGAs.

Although this report's emphasis is on package and assembly quality and reliability, device technologies and assurance methodologies are also of paramount importance. As semiconductor scaling continues, manufacturing large, defect-free integrated circuits becomes increasingly difficult with added further degradation during screening and use. Reconfigurability of FPGAs enables opportunity for fault tolerance development first by detecting faults and then by implementing mitigation approaches for the faults. Degradation and fault have many mechanisms, including the followings:

- Degradation due to a hot carrier induced (HCI) effect that leads to a buildup of trapped charges in the gate-channel interface region.
- Degradation due to negative biased temperature instability (NBTI), which exhibits similar to buildup of trapped charges.

- Degradation due to electromigration (EM) mechanisms, in which metal irons migrate over time leading to voids and deposits in interconnections, eventually causing faults due to the creation of open and short circuits.
- Degradation due to time-dependant dielectric breakdown (TDDB), which affects the gates of the transistor, causing an increase in the leakage current and eventually a short circuit.
- Fault due to manufacturing defects can be exhibited in circuit nodes as stuck, switch too slowly to meet the timing specification, or cause short or open circuit.
- Fault due to radiation exposures, including single event upsets (SEUs) and single event transients (SETs). The most commonly considered failure mode is the flipping of an SRAM cell in the configuration memory.

4. PBGA Reliability

4.1 Background

Reliability of plastic and ceramic ball/column grid arrays has been assessed as part of previous NEPP activities. The most critical variables incorporated in the various investigations have been package types (ceramic column/ball and plastic); board materials (FR-4 and polyimide); surface finishes (OSP, HASL, and Ni/Au); solder volumes (low, standard, and high); and environmental conditions.

Plastic BGAs with a variety of sizes and shapes are abundantly available and are used widely by commercial industry for a variety of applications from benign office environments to high-end server applications. Military and avionic industries are also using them selectively after they have reached an acceptable level of maturity. Because of their wider applications, reliability is generally characterized by the package suppliers and is verified by industry for specific applications. Numerous excellent publications and references are available through IEEE CPMT, SMTA, IMAPS, and IPC proceedings and journals such as the Microelectronic Reliability Journal.

This section categorizes assembly reliability for a number of plastic ball grid arrays (PBGAs) based on a literature survey. Reliability data from researchers as well as suppliers for FCBGAs are gathered in order to narrow the key parameters that affect reliability.

4.2 Plastic Package Assembly Reliability

Table 1 lists cycles-to-failure (CTFs) for a number of plastic packages with different configurations, selected from those reported in the literature [12–17]. Thermal cycle test results are for tin-lead balls with tin-lead solder, even though most recent data generated by industry are for lead-free balls/solder. Lead-free packages/solders are yet to be fully adopted for high-reliability applications. However, in order to update the literature survey and link the behavior of the two solder alloys, data for the full array PBGA 676 I/Os are compared in [10] and briefly discussed in Section 6 Test Results. The following paragraphs present the effect of a few key parameters on solder joint reliability.

Table 2 clearly shows the effect of thermal cycle range on CTFs: as delta T increases, CTF generally decreases. Maximum and minimum temperature and dwell time at these temperatures contribute to failures. For example, the CT1%F (cycles-to-one percent-failure) for PBGA 256 I/O and 1.27-mm pitch in the range of 0° to 100°C was more than 9000 cycles (case #2); it was significantly reduced to approximately 2000 cycles when the temperature range increased to –40°/125°C (case #11).

Package size, thickness, configuration, internal die attach type, and I/Os also play a significant role in CTF. For example, in comparing case #2 to case #3, a significant decrease in CT1%F is shown when package I/O increased from the 256 I/Os, 1.27-mm, to 1849 I/Os (>9000 vs. 3095 cycles in the range of 0 to 100°C). Note that package configuration is also different for the higher I/O package; it has flip-chip die rather than wire-bond die attachment.

Die size and its relation to package size and ball configuration affect PBGA packages, whereas it has a lower effect on ceramic ball grid array/ceramic column grid array (CBGA/CCGA) CTF. This is not apparent from the cases presented in Table 1, but the die

and package sizes are listed for identifying such correlation. The comparison of cases #7 and #8 indicates an increase in CTF when die size is increased. These results, contrary to general trends, may be due to the confounding effects of adding a heat sink for case #8. Package and failure information for a FCBGA with 1508 I/Os (case # 9) from the recent reliability report (Report 49 Q1 2010) is also added. During listing of the recent data, it was noticed that recent results for the FCBGA 1020 are different from the previous report. This author did not change what was reported in a previous literature review as listed in Table 1. For solder joint reliability of packages, readers should refer to most recent reports provided by package suppliers since package and board configurations affect reliability results.

Printed wiring board (PWB) thickness/stiffness also affects PBGA CTF. Preferred thickness was defined as 2.3-mm in IPC 9701 [18] since it is known that, generally, packages assembled on thinner PWBs show higher CTFs. It is difficult to show the effect of board thickness on solder joint reliability of PBGAs since most package suppliers now follow the IPC 9701 requirement for the board thickness and most low I/O packages survived a large number of cycles. For example, PBGA 256 I/O showed no failures to 9000 cycles (case #2); one reason may be the use of a thinner board (1.6 mm) rather than a thicker board (2.3 mm) specified by IPC for assembly and solder joint reliability testing.

Table 1. Cycles-to-failure data for tin-lead/tin-lead ball/paste illustrating the effect of a number of key variables.

Case No.	Package (I/O, pitch)	Pkg Size (die size, mm)	Thermal Cycle Condition (ramp, dwell, cycle/hr)	First Failure	Mean Life ($N_{63.2\%}$)	Comments
1	PBGA-119-1.27	27 × 27 ? (17.8 × 17.8 × 0.3)	0°C/100°C (10 min, 5 min, 2)	6260 (1% failure)	12215	27 Pkg Ref. Mawer [12]
2	PBGA-256-1.27	27 × 27 (10 × 10)	0°C/100°C (10 min, 5 min, 2)	No failure to 9000 cycles	No failure to 9000 cycles	PWB 1.6-mm Thk Ref. Amkor [13]
3	FCBGA-1849-1.27	??	0°C/100°C	3095 (1% failure	4710	Ref. Shiah [16]
4	PBGA-256-1.0	17 × 17 (8.80 × 7.9)	0°C/100°C (10 min, 5 min, 2)	3687 (1% failure)	N/A	Full Array PWB, 2.3-mm Thk Ref. Altera [14]
5	PBGA-676-1.0	27 × 27 (17.8 × 17.8 × 0.3)	0°C/100°C (10 min, 5 min, 2)	4686	6012	30/30 Fail, PWB, PWB 2.36-mm Thk Ref. Xilinx [15]
6	PBGA-900-1.0	31 × 31.5 (17 × 17 × 0.3)	0°C/100°C (10 min, 5 min, 2)	4405	5344	28/28 fail PWB 2.36-mmThk. Ref. Xilinx [15]

Case No.	Package (I/O, pitch)	Pkg Size (die size, mm)	Thermal Cycle Condition (ramp, dwell, cycle/hr)	First Failure	Mean Life ($N_{63.2\%}$)	Comments
7	FCBGA-1020-1.0	33 × 33 (22.6 × 19.9)	0°C/100°C (2 cycles/hr)	5670 (1% failure)	N/A	PWB Thk 2.3-mm 6 layer build up BT Pre-2010 data. 2010 failure data differ from earlier repot
8	FCBGA-1020-1.0	33 × 33 (17.9 × 16.7)	0°C/100°C (2 cycles/hr)	2770 (1% failure)	N/A	Pre 2010 failure data
9	FCBGA-1508-1.0	(40 × 40) (23.9 ×23.3)	0°C/100°C (2 cycles/hr)	2040 (1% failure)	3074	2010 failure data Ref. Altera [14]
10	PBGA-313-1.27	35 × 35 (13 × 13)	-30°C to 100°C (25 min, 15 min, 0.75)	3310 (1% failure)	4000	13 Pkg, PWB 1.6-mm Thk Ref. Evans / Ghaffarian [17]
11	PBGA-256-1.27	27 × 27 (10 × 10)	-40°C–125°C (15 min, 15 min, 1)	~2000 (1% failure)	3164	PWB 1.6-mm Thk Ref. Amkor [13]
12	PBGA-676-1.0	27 × 27 (17.8 × 17.8 × 0.3)	-40°C–125°C (15 min, 15 min, 1)	1341	1830	27/32 Fail, PWB 1.6-mm Thk Ref. Xilinx [15]

Double-sided, mirror-image PBGA assemblies have significantly lower CTF compared to their single-sided version. Table 2 shows an example of the effect of a double-sided mirror image on CTFs for a 175 I/O flip-chip package [5, 19, 20]. Recently, Chaparala, et al. [21] performed experimental and modeling analyses to verify results presented by Ghaffarian in his 1999 article published in *Chip Scale Review Magazine*. Ghaffarian reported that the mean time to failure for mirror-imaged CSP assemblies in thermal cycling is 40–60% less than that observed for single-sided CSP assemblies. He identified the factors differentiating double-sided assemblies from single-sided assemblies as an increase in assembly standoff due to a second reflow pass, an increase in assembly stiffness, and thermal disturbance due to the package on the other side of the PWB.

Table 2. Comparison of TV-2 FPBGA thermal cycle test results (–55°/125°C) to literature data for 0 to 100°C thermal cycle range.

TV ID	Board Thickness (NSMD pad size)	Via Location (diameter)	Thermal Cycle Range (total time)	Weibull Scale (no.)	Weibull Shape (m)	Accelera-tion Ratio
175 I/O FPBGA-enhanced Single-Side Condition 1 *Condition 2*	1.57 +/−0.2 (300 μm) *(400μm)*	On pad (125 μm)	0°C to 100°C (32 min)	4331 3525	11.1 9.1	N/A
175 I/O FPBGA-standard Double-Side Condition 1 *Condition 2*	(300 μm) *(400μm)*	N/A	N/A	1616 1163	17.6 10.5	N/A
TV-2 175 I/O FPBGA 9 data points 8 data points	1.27 (300 μm)	On pad (100 μm)	−55°C to 125°C (68 min)	1126 1134	6 11.9	3.8

5. Experimental Approaches

5.1 Package and Assembly Variables

The purpose of this aspect of the investigation was to characterize the reliability of FCBGA and PBGA packages with I/Os in the range of 1500 to 2500. Test vehicles (TVs) were built with daisy-chain FCBGA packages with 1704 I/Os and 1.0-mm pitch, FPBGA packages with 432 I/Os and 0.4-mm pitch, and a control PBGA package with 676 I/Os and 1.0-mm pitch. Figure 3 shows a photomicrograph of a section of ball pattern of FCBGA1704 package (left) and daisy-chain design pattern for the all-ball connections and probe pads for local global and local monitoring. As apparent in a few locations, daisy-chain patterns were not in a regular pattern, showing an irregular jumper that needed to be verified through probing of assigned balls prior to committing to building printed circuit boards. Visual inspection of the package by microscope revealed that these irregular daisy connections were on the surface of package and therefore could be identified visually as marked on the photomicrograph. Figure 4 shows the board design with daisy-chain pattern and routing of traces to the edge of the board for daisy-chain monitoring.

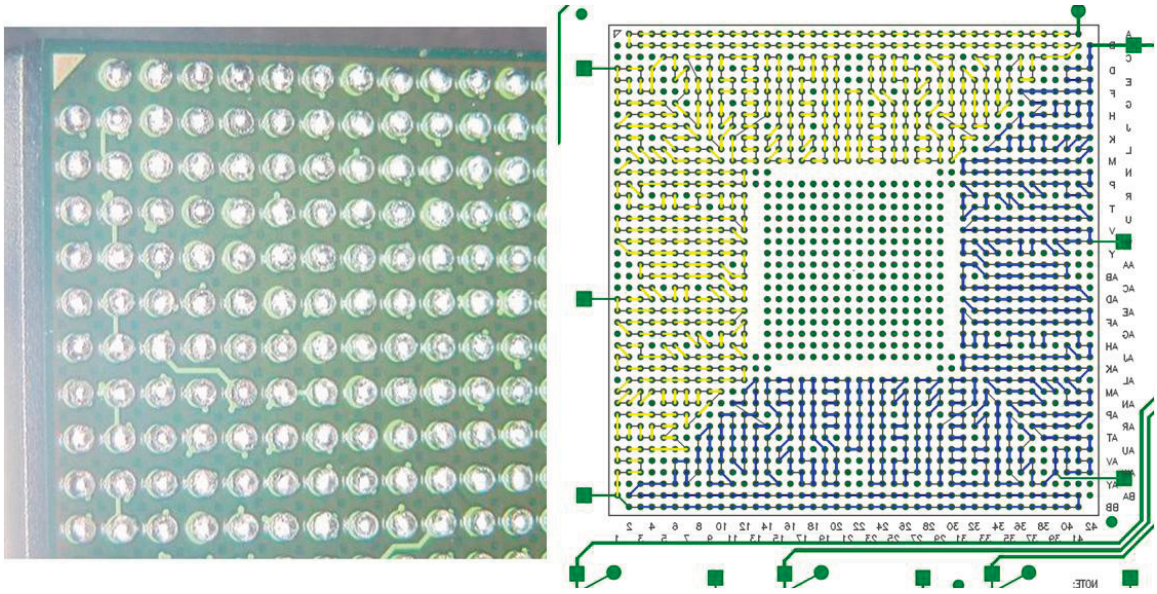

Figure 3. Photomicrograph (left) and daisy chain pattern 0f 1704 I/O flip-chip BGA (FCPBA) with 1.0-mm pitch and 42.5-mm^2 body size.

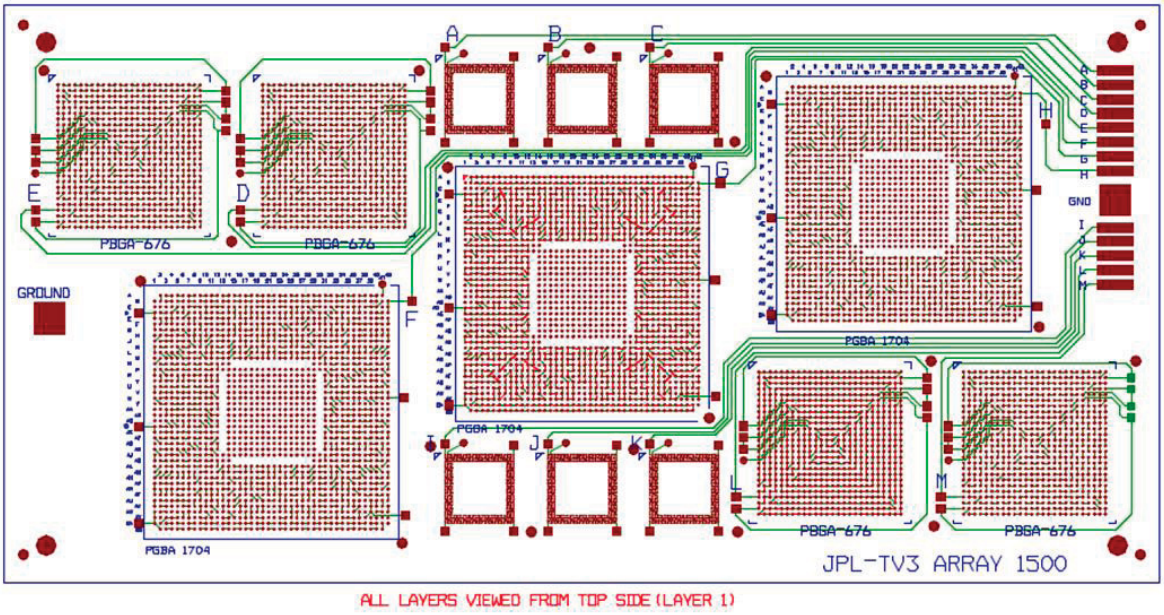

Figure 4. Test vehicle design showing combined package and board daisy-chain patterns at three locations for the 1704 I/O flip-chip BGA (FCPBA) package with 1-mm pitch and 42.5-mm^2 body size. Location and board daisy-chain patterns for PBGA 676 I/Os and 432 I/Os are also apparent in the design.

A design of experiments (DOE) technique was used to cover various aspects of processing and packaging assembly reliability. The following packages and parameters were evaluated as part of a larger DOE implementation:

- The FCBGA1704 with 1.0-mm pitch and 42.5-mm^2 body size designed in three locations, one at the center with high sensitivity to mechanical loading. Numerous daisy chains were designed on board to compliment daisy chains on a package in order to generate complete chains for solder joint failure monitoring. Probe pairs were added near packages to monitor subdivided daisy chains.
- Six 432 I/O FPBGAs with 0.4-mm pitch and 13-mm^2 body size as well as four 676 I/O PBGAs with 1.0-mm pitch and 27-mm^2 body size were included in the evaluation.
- Boards were made from high glass transition temperature (Tg) FR-4 materials with 0.093-inch thickness. They had a hot air solder leveling (HASL) tin-lead surface finish commonly used for tin-lead solder.
- A standard 4-mil-thick stencil was used for paste printing of the whole board. However, a mini stencil with 4-mil thickness was used for paste printing locally when it was required to accommodate assembly of FCBGA1704 packages by a rework station.
- Solder paste volumes were measured at the four corners and at the center for several assemblies to document actual paste print volume, distribution, and solder paste release efficiency.

- Vapor phase reflow was used to assemble all packages, including the 1704 I/Os when it was required as part of the DOE design. Only the FCBGA1704 packages were also assembled using a rework station as required by design.
- A number of FCBGA1704 packages were mechanically strengthened by applying spot bond adhesives at the corners and centers after assembly. A test vehicle was conformally coated.

These assemblies were first subjected to inspection and daisy-chain continuity checks to determine manufacturing robustness of various package configurations. They were then exposed to a number of environmental conditions to evaluate their reliability and failure mechanisms. Both the process yield and reliability results for FCBGAs, FPBGAs, and PBGAs are discussed below.

5.2 Test Vehicles and Assembly Parameters

Figure 5 shows a test vehicle assembly with one 1704 I/O, six 432 I/O FPGAs, and four 676 I/O PBGAs. All boards were laminated from a high Tg FR-4 epoxy having 4×6 inch surface area and thickness of 0.093 inch as specified by IPC 9701. All packages had daisy chains where most pairs of pads were connected internally within the die and a few connected through exposed traces. Complementary pairs of PWB pads were designed so that their connections within package daisy chain pairs completed a specific daisy-chain pattern for solder joint failure monitoring. Daisy chains for each package were used for monitoring at intervals to detect failures due to either thermal cycling or drop tests. Additional small probing pads were added at each side of the package for manual probing in more detail, enabling further narrowing of failure locations.

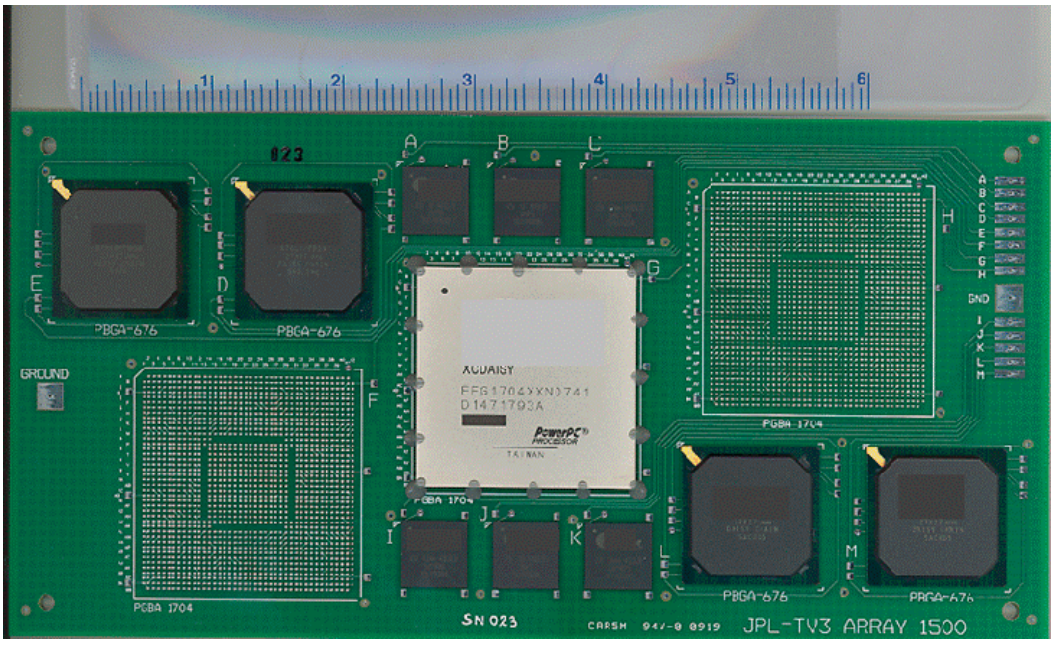

Figure 5. Photomicrograph of a partially populated test vehicle showing the spot staking of the FCBGA1704 at the corners and periphery.

5.3 Solder Paste Volume

Initially, type III (−325+500) RMA pastes, solder particle diameter between 25 and 45 microns, were used for paste deposition on the PCB pad's patterns using a paste print machine with standard parameters, including paste print speed. Later, type V (−500) RMA paste, solder particle diameter between 15 and 25 microns, was used to improve assembly yield for fine pitch BGA parts. The rule of thumb for an aperture opening is for it to be about four to five times the solder powder diameter. After deposition, each paste print was visually inspected using a microscope for detecting gross defects such as bridging or insufficient paste deposition. For the FCBGA1704, on rare occasion, print quality was improved by either adding a small amount of solder paste when insufficient paste was detected or by removing solder paste from the connecting pads when bridging was discovered. Figures 6 and 7 show representative photomicrographs of paste print and quality for the FCBGA1704 and the FPGA432, respectively.

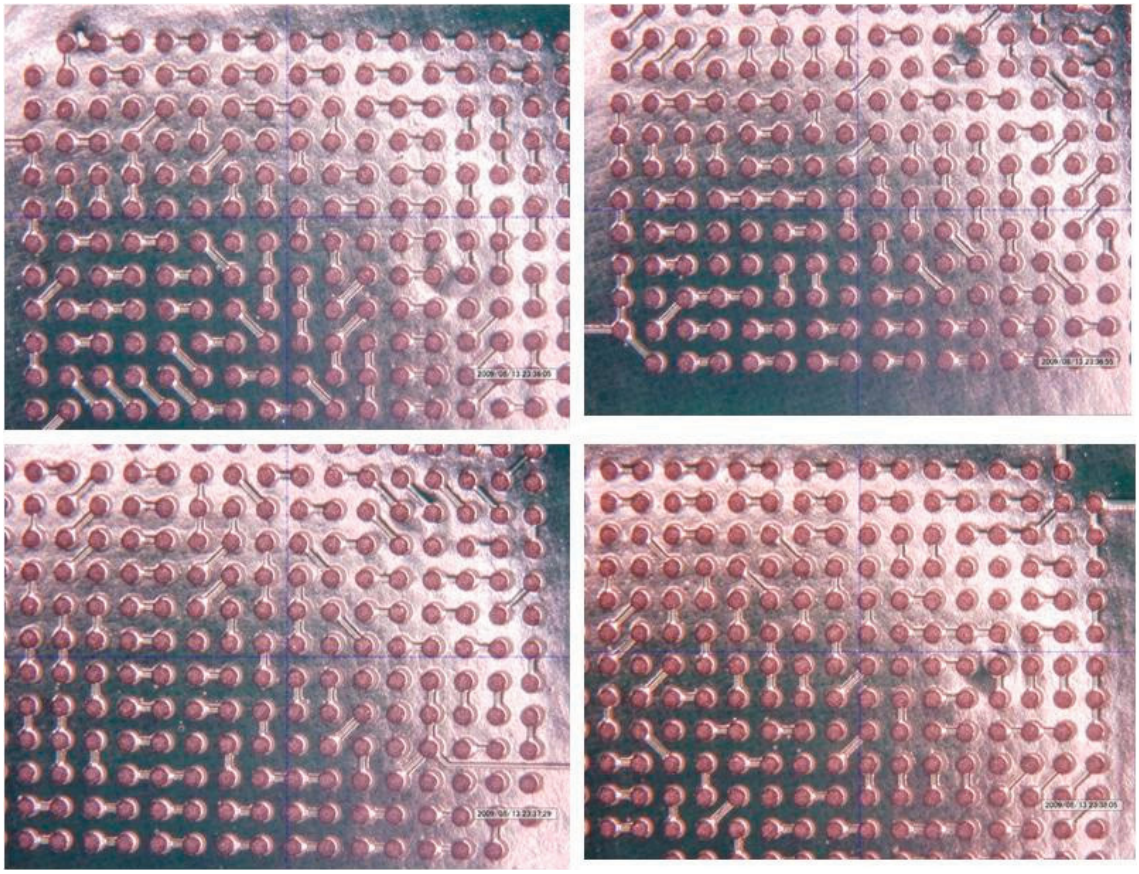

Figure 6. Representative photomicrographs of paste print deposition quality for the FCBGA1704 pattern on PWB.

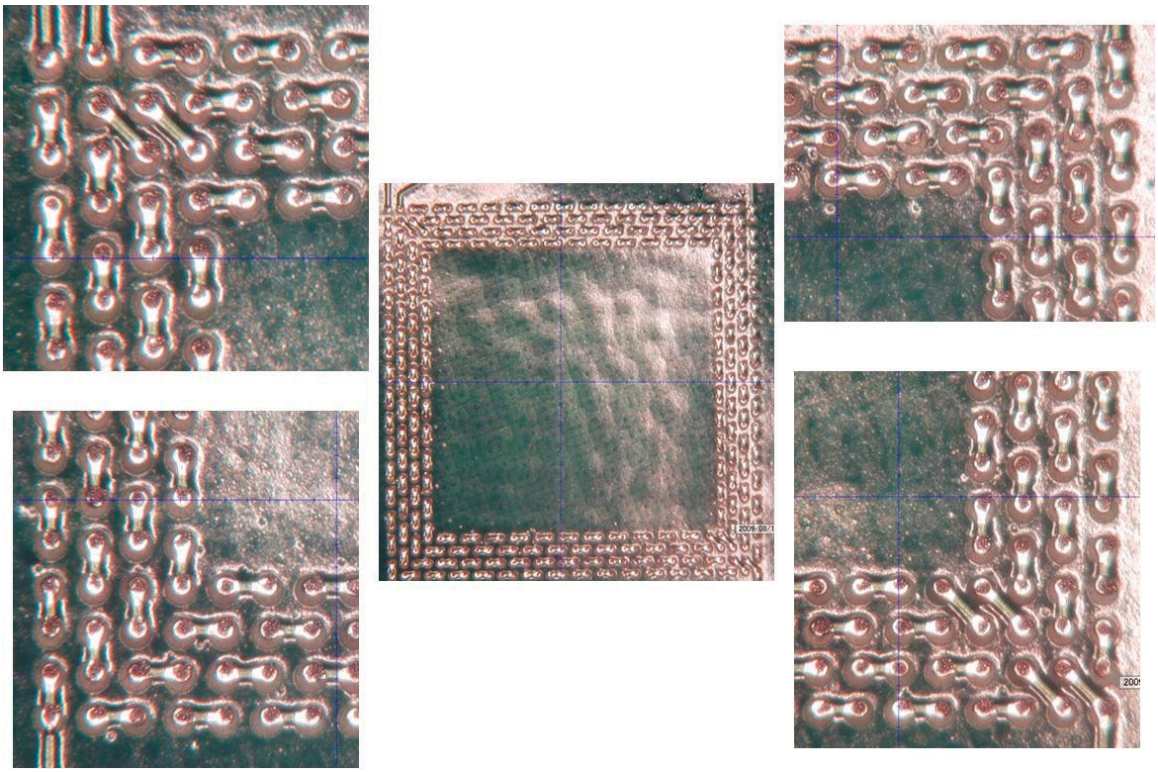

Figure 7. Representative photomicrographs of paste print deposition quality for the FPGA432 pattern on PWB.

In addition, solder paste areas and heights were measured using a laser profilometer with a three-dimensional (3D) measurement capability. Measurements were made at numerous locations—including corner and peripheral center pads—to gather solder volume data and their corresponding distributions.

Figure 8 shows an example of photomicrographs of FCBGA1704 pads after solder paste deposition quality and solder paste characteristics parameters, including heights and areas. This figure also shows color-coded height distribution of solder paste print for this set of pads. A similar distribution with acceptable quality was achieved for solder paste deposition of PBGA676 with 1.0-mm pitch. Overall, no major manufacturing issues were encountered with the paste depositions for the two BGAs with 1.0-mm pitch.

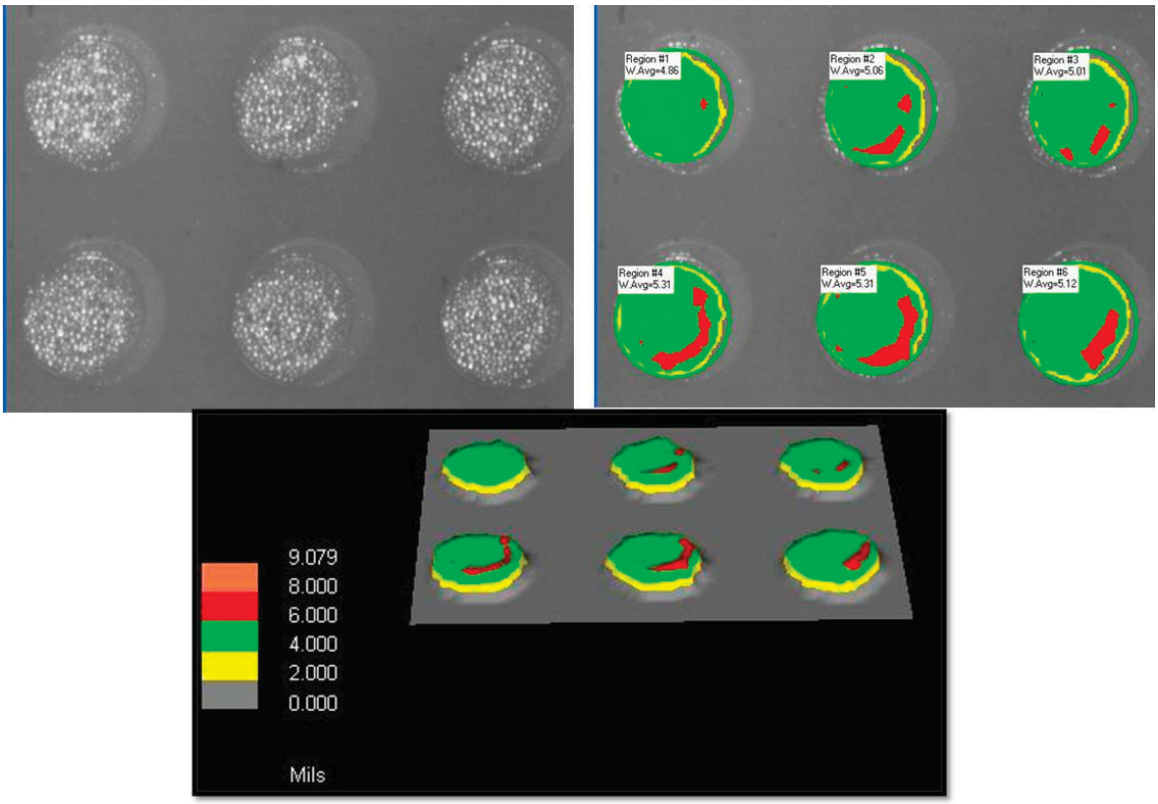

Figure 8. Solder paste print quality and estimated volumes for FCBGA1704 using a laser profilometer. Color-coded solder height distribution (bottom) can also be seen.

Figure 9 shows an example of photomicrographs of solder paste print and color-coded height for the FPBGA432. Uneven distribution of solder pastes is apparent especially from color-coded figures. The variation shown for solder paste print quality was considered unacceptable when type III solder paste was used. Use of solder type III was discontinued after a few trial paste depositions. Type V solder paste was used after initial trial with some improvement. Figure 10 shows representative plots of solder paste distribution and color-coded heights for the FPBGA432 package using the type V solder paste.

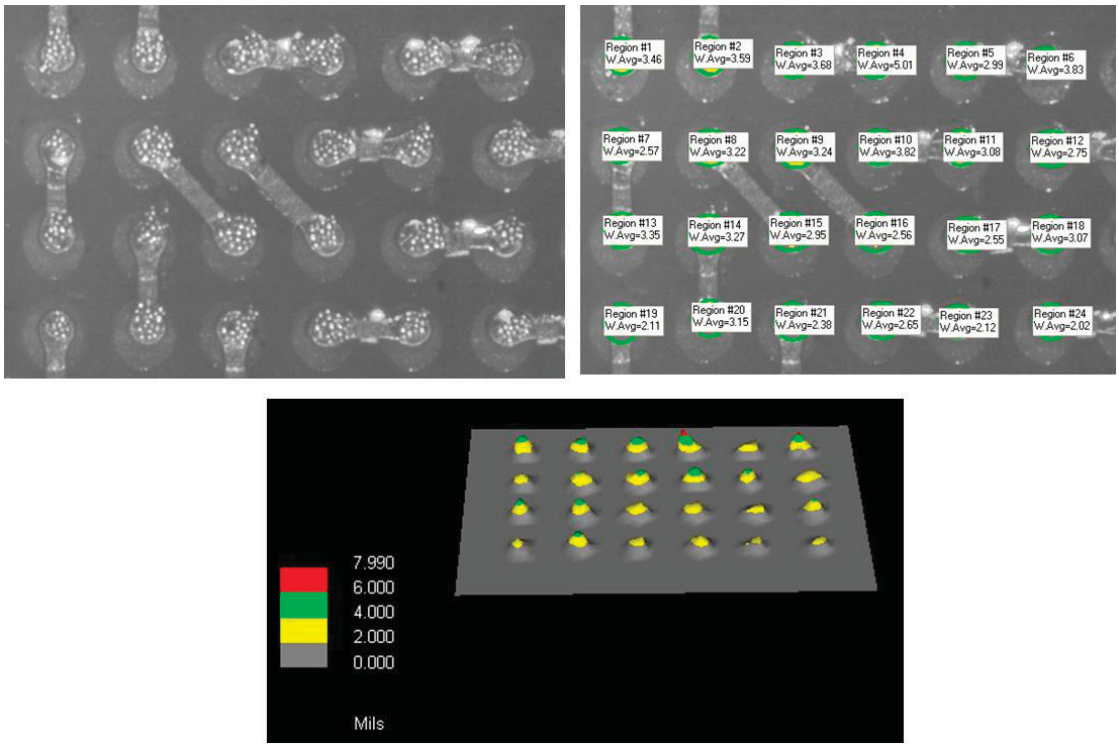

Figure 9. Examples of plots of solder type III paste print quality and volumes for FPGA432 using a laser profilometer.

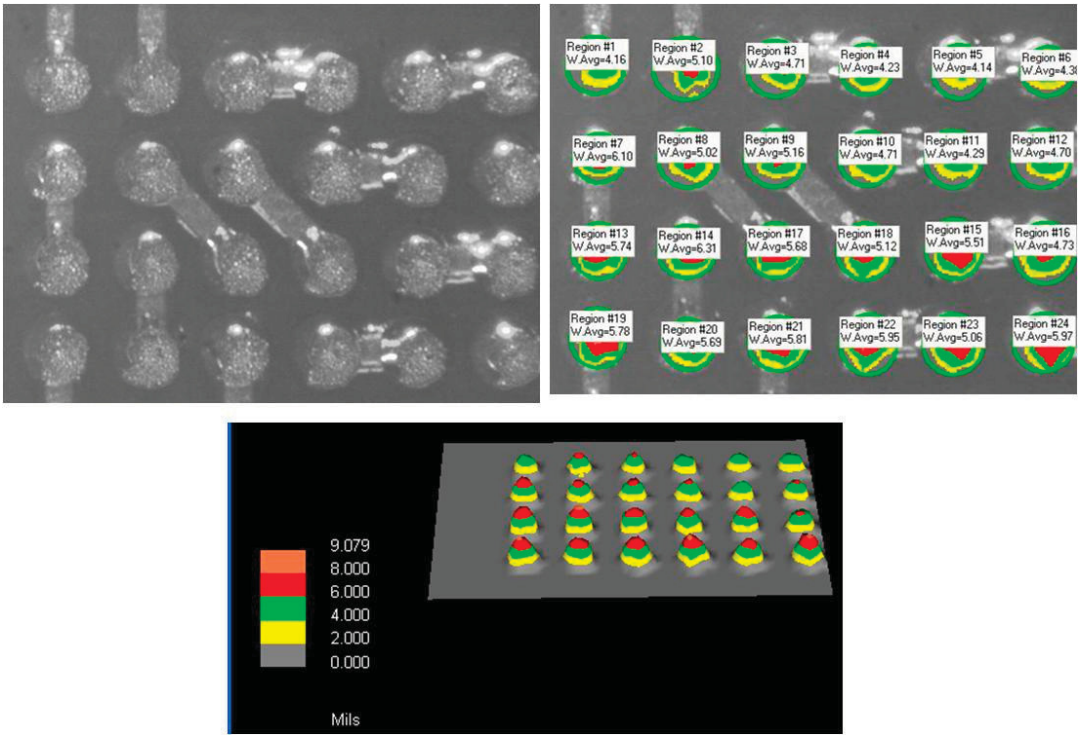

Figure 10. Examples of plots of solder type V paste print quality and volumes for FPGA432 using a laser profilometer.

5.4 Attachment Procedures

Intentionally, a large number of FPGA432 packages were designed close to the FCBGA1704 package. The reason for such configuration was to determine paste print quality and manufacturing challenges associated with a large array package surrounded by small fine pitch ones. As envisioned, significant processing challenges were encountered during assembly. These were further aggravated in some cases where the package had lead-free solder balls that were assembled with tin-lead solder paste. To minimize solder bridging of FPGA432, a 4-mil-thick stencil was used for both standard and mini stencil paste printing. Appropriate aperture opening size for each package type was designed to achieve a minimum level of solder paste volume.

Initially, type III with coarser solder powders was used, but it was thought that the use of type V solder paste with a finer mesh should improve manufacturability and yield for the fine pitch BGA packages. Package placement was accomplished using an automatic placement machine. However, placement by rework station was also performed to determine feasibility of such approach.

Solder paste reflow was performed using a vapor phase reflow machine set up for tin-lead process. Reflow profiles were based on a previously established profile that was tailored using a sample run with the attached thermocouple generating the reflow thermal profile. Vapor phase consists of an infrared preheating followed by a constant temperature boiling vapor zone. Infrared preheating temperature and time as well as time in vapor phase are the only key parameters that can be modified to achieve better solder attachment quality. For the FPBGA1704, mini stencil was used for paste printing and rework station for package placement and solder reflow.

5.5 X-ray

Real time x-ray systems are categorized as 2D and 3D x-ray systems. The 2D system is a standard x-ray inspection system with a microfocus source and a stationary image intensifier as the detector, capable of producing offset pseudo 3D features. The 2D system utilized has stationary microfocus source intensity, but the detector had off-axis rotational capability. The transmission x-ray captures everything between the x-ray source and image intensifier since x-rays are emitted from the source and travel through the sample. The higher the density of the sample (e.g., solder balls in PBGAs), the fewer x-rays will pass through and be captured by the image intensifier. The detected x-rays are displayed in a grayscale image, with the lower density (such as voids) areas appearing brighter than the higher density areas. The voltage and current of the x-ray's intensity can be adjusted to reveal features of most sections of the sample.

The 2D x-ray systems are very effective in testing single-sided assemblies. With the use of a sample manipulator, an oblique view angle enhances inspection of both single and double-sided assemblies with some loss of magnification due to increase in distance between source and detector. Experience is needed in discerning between bottom-side board elements and actual solder and component defects. This can be very difficult or even impossible on extremely dense assemblies. In any case, only certain solder-related defects such as voids, misalignments, and solder shorts are easily identified by transmission systems. However,

even an experienced operator can miss other anomalies such as insufficient solder, apparent open connections, and cold solder joints.

The x-ray system with a rotational detector allows oblique generation of x-ray images with a higher magnification and a better intensity resolution since the focal spot remains the same and there is, therefore, no loss of magnification. An isocentric manipulator keeps the field of view unchanged when the oblique view mode is used. This feature allows better characterization of some defect features, including wettability and void location in area array packages.

5.6 Thermal Cycle Test Profiles

Three different thermal cycles were used with the following thermal profiles:

1. Cycle A: Ranged from –55° to 100°C with a 2° to 5°C/min heating/cooling rate. Dwells at extreme temperatures were 15 minutes.
2. Cycle B: Ranged from –55° to 125°C with a 2° to 5°C/min heating/cooling rate. Dwells at extreme temperatures were at least 10 minutes with duration of 159 minutes for each cycle.
3. Cycle C: Ranged from –125° to 125°C with approximately 5°C/min heating/cooling rate and 10-minute dwells.

Because of limited sample size, in some cases test vehicles were first exposed to harsher thermal cycles to ensure their integrity in short time, then followed up with a milder thermal cycle for longer time exposure evaluation. The criteria for an open solder joint specified in IPC-9701A were used as guidelines to interpret electrical interruptions. Opens were manually verified at convenient intervals.

6. Test Results

6.1 Daisy-Chain Resistance Results

As the first step, daisy-chain resistances for package assembly were measured after first and subsequent builds to verify process acceptance. All packages had a pair of connected pads, which complemented specific pairs of PWB pads to build loops of continuous daisy chains for solder joint opens. A short could be detected when lower-than-nominal resistance values were measured. The results of manufacturing yield for various conditions of assembly using vapor reflow and rework station are summarized in Table 3. Manufacturing yield for FCBGA1704 was favorable with only one open whereas this was not the case for the other two packages. The FPBGA432 showed unacceptably low yield while results for PBGA676 were mixed with medium to high yield.

Table 3. Summary of daisy-chain resistance measurements after build and in some cases after local reflow by rework station.

ID with Process-Environment	A 432- SnPb	B 432 SnPb	C 432 SAC105	D 676 SnAg	E 676 SnPb	F 1704	G 1704	H 1704	I 432SAC 305	J 432 SnPb	K 432 SAC405	L 676 SAC305	M 676 SAC405
SN01-Tv3-Vap-CF-Nbnd-JM	Open	Open	Open	2.1	Open	NP	6.9	NP	Open	3.2	Open	2.1	1.9
SN02-Tv3-Vap-16bnd-RIT	0.3	Open	Open	2	2.1	o	6.1	Open	1	0.8	0.9 ((AR)	2.1	2.1
SN03-Tv3-Vap-16bnd-JM	0.6 (AR)	0.1 (AR)	0.6 (AR)	1.8	1.9	NP	6.8	NP	NP (AR)	0.5 (AR)	0.2 (AR)	1.7	1.6
SN04-Tv3-Vap-Nbnd-RIT	0.9	0.7	0.7	1.9	2.1	NP	6.6	NP	0.8	0.7	0.7	1.7	1.6
SN05-Tv3-Vap-16bnd-JM	0.1 (AR)	0 (AR)	0.6 (AR)	1.5	1.8	NP	6.3	NP	np	NP (AR)	0.6 (AR)	(R/R)	1.3
SN06-Tv3-Vap-16bnd-RIT	1	0.9	0.9	1.9	1.9	NP	6.9	NP	1	0.9	0.9	1.9	2
SN07-Tv3-Vap-Nbnd-JM	0.4	0.1	Open	2	1.9	NP	6.3	NP	np	0.2	Open	1.9	Open
SN-10-TV3-3Pt/LLC-LFll-Vap-Nbnd-JM	1.2	1.2	1.1	2.4	2.5	Open (AR)	7	6.4	0.9	0.8	0.9	1.9	Open (RR)
SN11-TV3-RWK-TL-TL;Nbnd-JC	0.8	0.7	0.7	1.7	1.7	NP	6.6	NP	0.8	0.8 (AR)	0.8	1.7	2.2
SN12-TV3-RWK-TL-TL;16bnd-RIT	0.6	0.6	0.7	1.7	1.8	NP	6.8	NP	0.7	0.7	0.7 (AR)	1.8	1.8
SN13-TV3-RWK-TL-TL;16bnd-RIT	0.7	0.7	0.7	1.8	1.9	NP	6.3	NP	0.8	0.7	0.7	Open	1.7
SN21-TV3-Vap-LF-TL-Nbnd-RIT	0.7	Open	0.7	1.8	2	Open	5.3	NP	0.6	0.6	0.6 (AR)	1.5	1.4
SN22-TV3-Vap-LF-TL-Nbnd-JC	1.2	0.6 (AR)	1.1	2.4	2.5	NP	5.7	NP	1.2	0.4 (AR)	1.1	2.2	10.8
SN23-TV3-Vap-LF-TL-16bnd-JC	0.4	0.2 (AR)	0.8 (AR)	1.7	1.7	NP	6.8	NP	9.5	0.3	0.7 (AR)	1.6	1.6
SN24-TV3-Vap-LF-TL-16bnd-RIT	0.7	0.7	0.7	2	2.2	NP	6.2	NP	0.9	0.8	0.8	1.7	1.7
Manufacturing Yield	Low	Low	Low	High	High	NA	High	NA	Low	Low	Low	Med	Med

AR Airvac reflow 2nd time
R/R Rework/Replace
NP No part to begin with

6.2 Inspection after TV Build

For high-reliability electronic applications, visual inspection is commonly performed by quality assurance (QA) personnel at various levels of packaging and assembly, known as mandatory inspection points (MIPs). Solder joints are inspected and accepted or rejected based on specific sets of criteria establish for high-reliability applications. Further assurance is gained by subsequent short-time environmental exposure, including thermal storage, thermal cycling, vibration, mechanical shock, and so forth. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level. For space applications, generally 100% visual inspection is performed for the hybrid package pre-sealing (pre-cap) and after assembly prior to shipment. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level. For

space applications, generally 100% visual inspection is performed for the hybrid package pre-sealing (pre-cap) and after assembly prior to shipment.

For PBGA package assembly, visual inspection is of limited use since it is difficult to inspect peripheral ball interconnection and impossible to inspect hidden balls under the package. X-ray evaluation is needed for area array packages to determine shorts and possibly opens in a rare occasion. For the test vehicle with daisy-chain package configuration, verifications were performed: (1) through daisy-chain continuity checking and (2) through x-ray quality detection for shorts and in a rare occasion for opens. For the FPGA432 assemblies, shorts were clearly detected by x-ray and gross opens in some cases apparent by being much smaller size balls. In a few cases, open and package lift was even apparent under optical microscope. To reduce cost, representative quality was verified by cross sectioning only after environmental tests.

6.3 X-ray Characterization

6.3.1 After Assembly

X-ray inspection followed the daisy-chain continuity check to selectively verify package/assembly conditions. The 2D real time x-ray transmission system with up to 70° oblique angle views was utilized for this inspection. Figure 11 shows representative x-ray photomicrographs for the FPBGA432, marking a potential open with an arrow. Figure 12 shows additional x-ray photomicrographs with arrows pointing to shorts and potential opens.

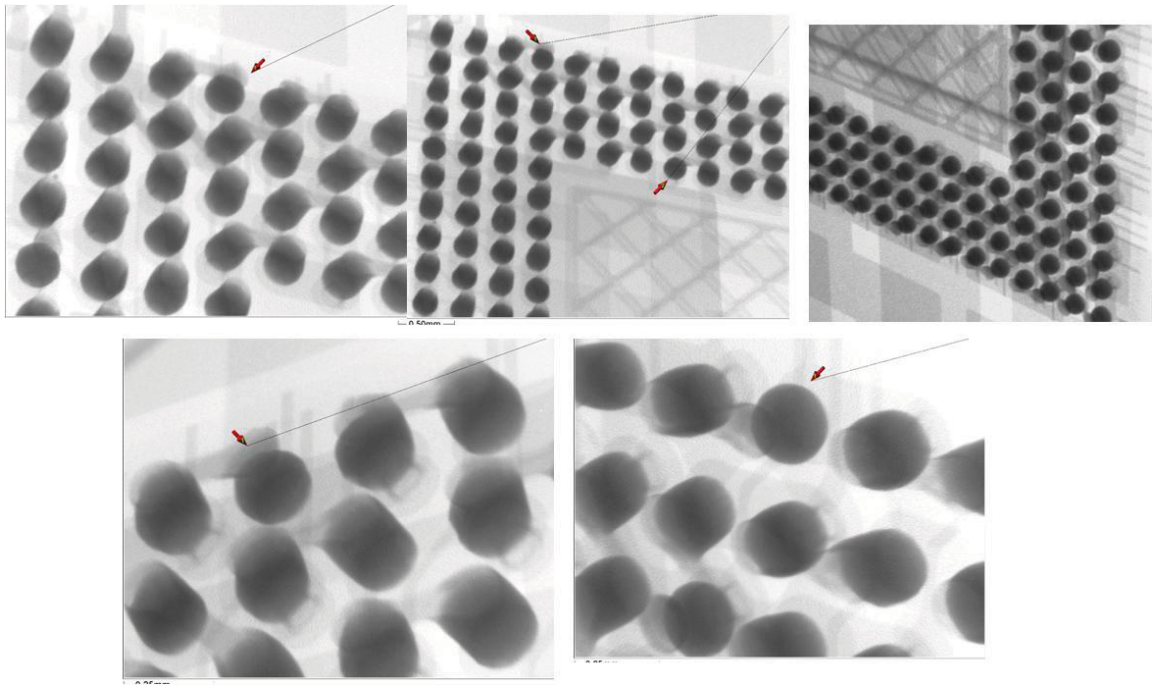

Figure 11. As-assembled X-ray photomicrographs for the FPGA432 attachments.

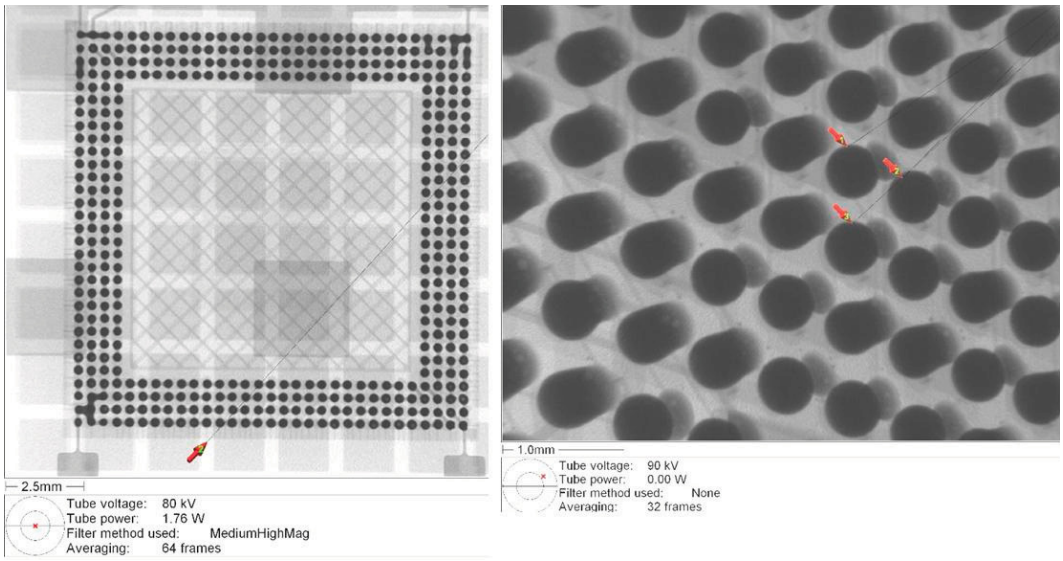

Figure 12. Representative as-assembled x-ray photomicrographs for FPGA432 attachments showing shorts (left) and open conditions.

The x-ray of PBGA676 shown in Figure 13 showed minimum voids with no apparent shorts or opens. Only one test vehicle was fully evaluated prior to thermal cycling. A comprehensive x-ray evaluation of all assemblies may have revealed defects in rare occasions similar to those observed for the FPBGA432 packages. This statement is given based on inconsistency in daisy-chain resistance values for the PBGA676 package assembly.

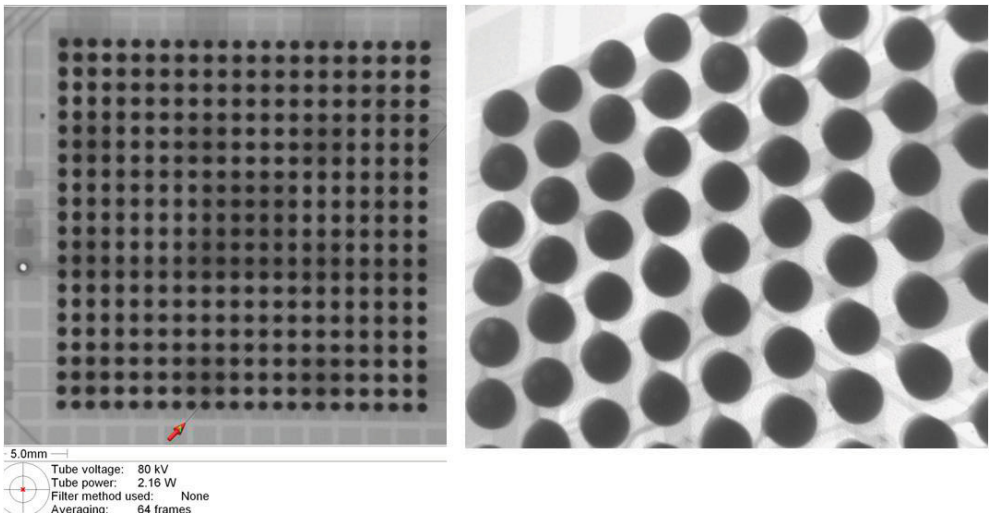

Figure 13. As-assembled x-ray inspection of PBGA676.

6.3.2 After Thermal Cycling

X-ray evaluation was also performed after temperature cycling for two assemblies when one of the FCBGA1704 packages revealed a daisy-chain open. A representative x-ray of the test vehicle for all parts laid on over their respective packages is shown in Figure 14. These x-ray photomicrographs further confirm the previous findings after assembly for the 432 I/O FPBGA packages. It also revealed shorts and potential opens due to manufacturing challenges for fine-pitch BGA surrounding the large FCBGA1704 package. For this specific test vehicle, only one out of four PBGA676 packages revealed open (location M) by daisy-chain continuity test after assembly. For this case, the daisy-chain continuity test result is in agreement with x-ray findings. However, daisy-chain continuity failure after thermal cycling identified for the FCBGA1704 could not be verified through x-ray evaluation at lower magnification. Further evaluation was carried out at a much higher x-ray magnification to determine if clear indication of failures could be identified. Figure 15 shows a representative x-ray of the top-right corner of packages at higher magnification, revealing more detail of shorts and potential opens where applicable. Figure 16 shows an x-ray of the FCBGA1704, location F, where failure was identified through daisy-chain evaluation. Again, no apparent damage or cracking was detected by x-ray. The photomicrographs, however, showed clearly the levels of voids—key advantage of x-rays—for solder balls and solder joints.

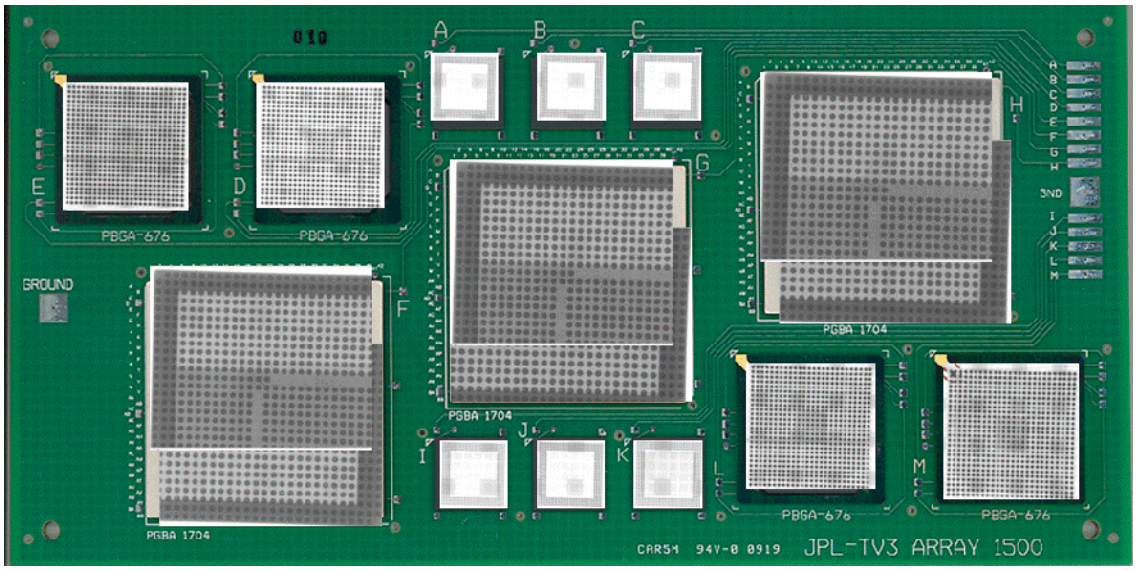

Figure 14. X-ray of package assemblies after thermal cycling laid over their respective packages showing their array configuration.

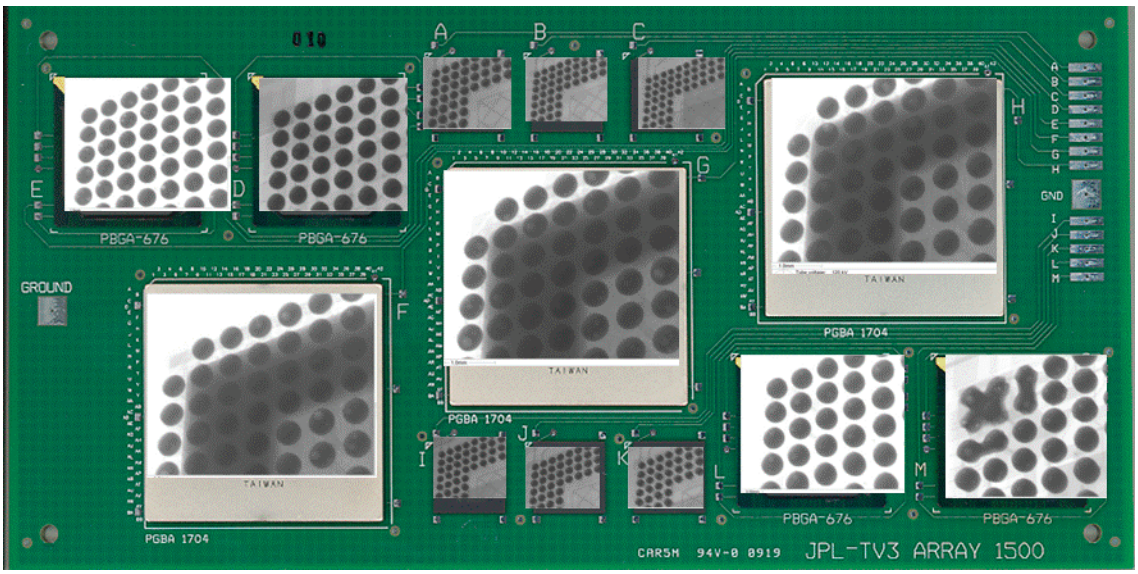

Figure 15. X-ray of package assemblies after thermal cycle showing only the top right corner balls at high magnification for better representing damage and anomalies.

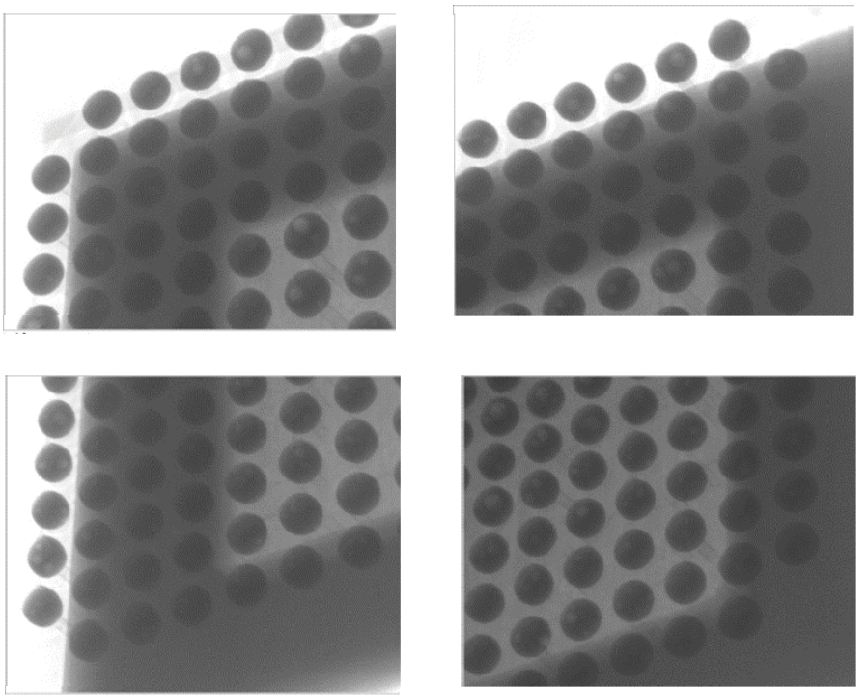

Figure 16. X-ray of FCBGA1704 package assemblies after thermal cycle showing the corner balls at higher magnification for better representing damage and anomalies due to cycling. No damage could be detected, but it shows levels of voids. Note that this package showed daisy-chain open after cycling.

6.4 SEM Microscopy Characterization

Contrary to conventional package assemblies where solder joints can be inspected by optical microscopy at intervals during thermal cycling, this is not the case for FCBGA packages that require accessibility to periphery solder balls and special optical microscopes. The only known approaches are package/board daisy-chain development for monitoring or destructive test by dye-and-pry and x-sectioning evaluation. These approaches are not foolproof either since failure other than solder joint may cause false detection. Because of x-sectioning a limited number of balls, this destructive technique provides only damage indicators for those balls' x-section, which generally may also be representative of other balls.

After failure detection by daisy-chain monitoring, scanning electron microscopy (SEM) evaluation was performed. In addition, elemental analysis was performed using dispersive x-ray spectroscopy (EDS) to obtain semi-quantitative elemental results for the flip- chip solder alloys and interface interconnections. A representative FCBGA1704 specimen was cut from the TV, close to the package edge, in order to be able to mount the specimen on the SEM mounting fixture and rotate the sample for full characterization at higher magnifications. Figure 17 shows representative SEM photomicrographs for a ball of FCBGA1704 package prior to cross-sectioning at various magnifications. Solder alloy phases are revealed through using the backscatter feature of the SEM microscope. No gross microcracks, either within the balls or at the package interfaces, are apparent. For the flip-chip BGA, the outer rows may or may not represent the most severe stress condition; therefore, the SEM photomicrographs evaluation may possibly not be representative of internal damage, especially for ball interconnections at the package die periphery.

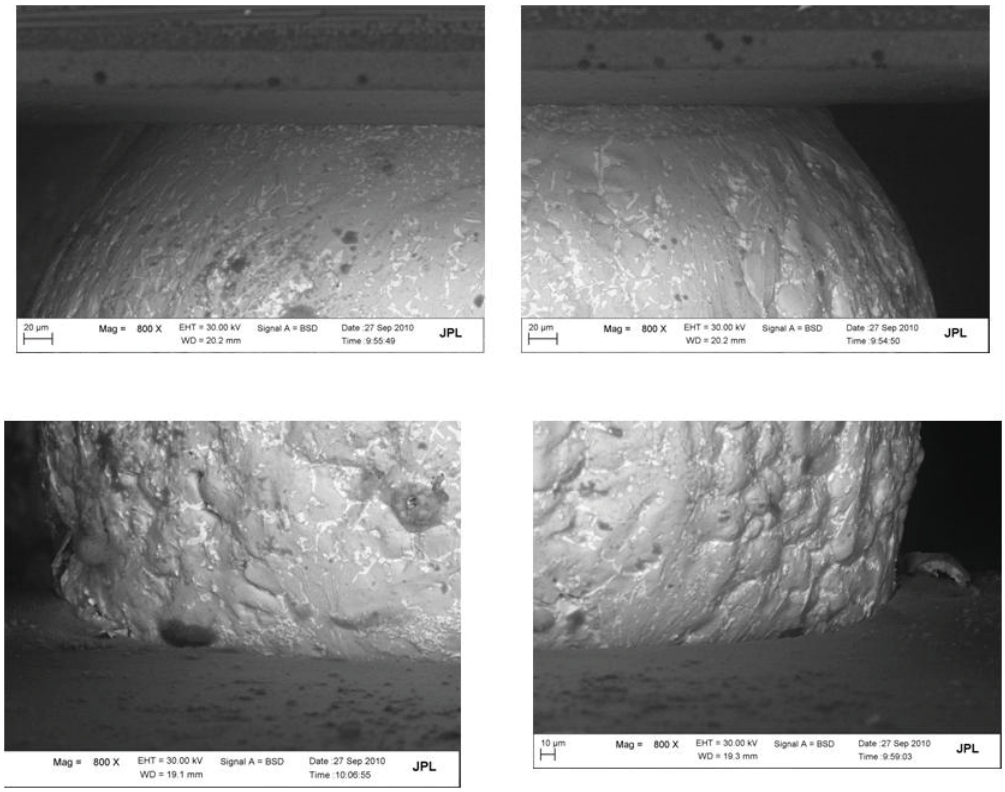

Figure 17. SEM photomicrographs of a FCBGA1704 solder after thermal cycling and prior to cross-sectioning.

6.5 X-sectional Verification

After initial SEM evaluation, x-sectioning was performed diagonally through the center of the FCBGA1704 package in order to reveal substrate lay-up structure, heat sink attachment feature, flip-chip solder and underfill integrity, and solder interconnection damage levels at the package and board interfaces. Heat sink and lay-up configurations, including die and substrate thicknesses, affect board level thermal cycle reliability and therefore are characterized. Figure 18 shows a representative SEM photomicrograph of an x-sectioned FCBGA1704 package showing measurement values for various sections of the package, including flip-chip balls at the die and flip-chip balls at the package/board level. Flip-chip solder balls are much smaller than those at the package level and have about a four times lower gap than the BGA balls. It is also apparent that high-density substrate with two layers of filled microvias were employed for transition of low pitch flip-chip at the die level to the higher pitch at the package level.

Flip-chip solder ball alloy compositional uniformity within solder and at the die and substrate interfaces is shown in Figure 19. There is no apparent degradation after a number of thermal cycles even though daisy-chain open is detected. Microvias shown in the figure also appear to show no degradation. The underfill under the die appears to show minimum degradation.

Figure 20 shows SEM photomicrographs of package solder balls and their interface integrity at the board and package interfaces. Note that the solder encloses the pad on the board since the board was designed as non-solder mask defined (NSMD) condition. This is not the case for the package that had a solder mask defined (SMD) pad. In addition, lead from tin-lead solder paste had diffused away from the board pad into the lead-free solder ball. It is not known whether this condition existed after assembly or tin-lead solder initially was segregated from lead-free alloy and lead was diffused later during thermal cycling.

Figure 21 shows x-ray elemental analysis along the center line of the package solder balls whereas Figure 22 shows x-ray elemental mapping for the solder ball. Elemental mapping for each element such as tin and lead are obtained through an EDS scan and are presented as different color intensity for visual observation. The solder is heavily distributed with tin having a minimum level of copper that is scattered throughout the solder ball. The silver element has to be accumulated specifically since it had no visual appearance; it was calculated to be about one percent, which is much lower than the expected four percent based on the SAC405 lead-free alloy composition.

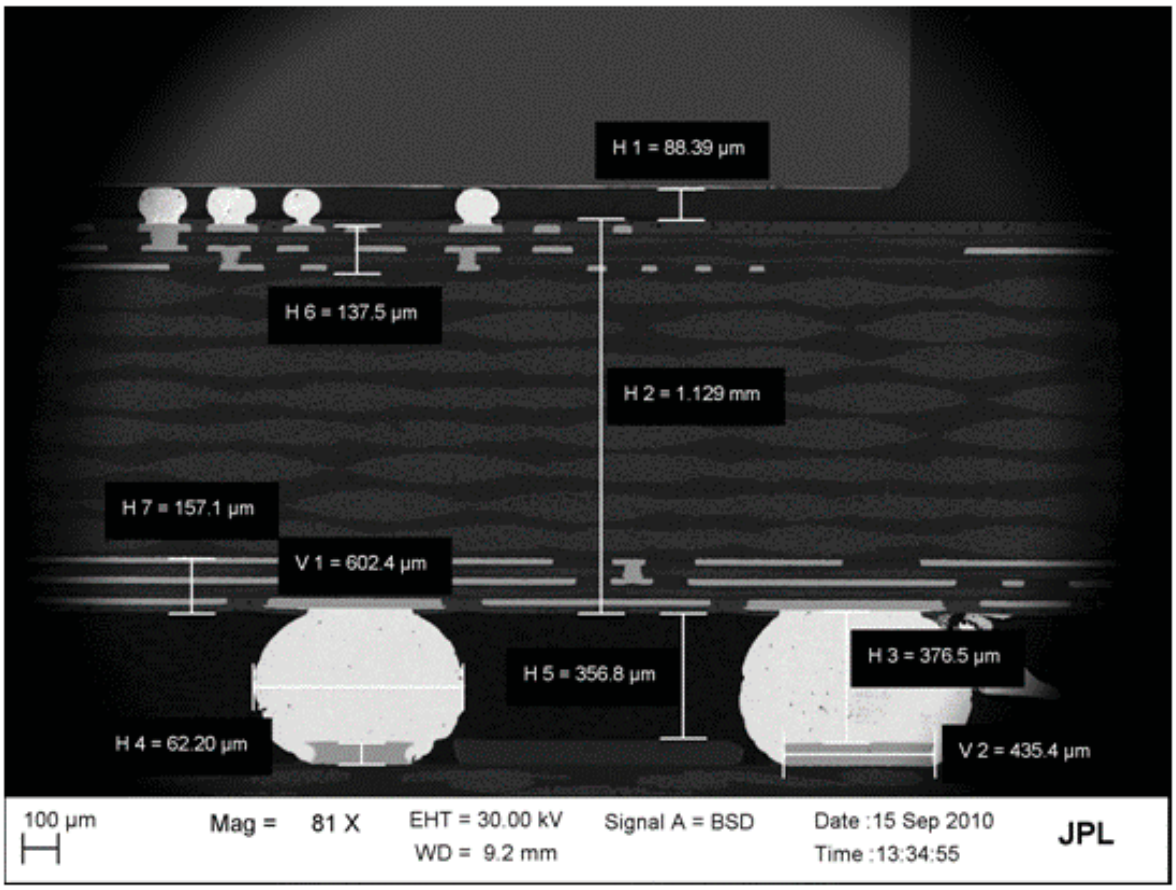

Figure 18. Cross-sectional photomicrograph of FCBGA1704 assembly after thermal cycling showing flip-chip balls at the die and at the package/board levels and their sizes.

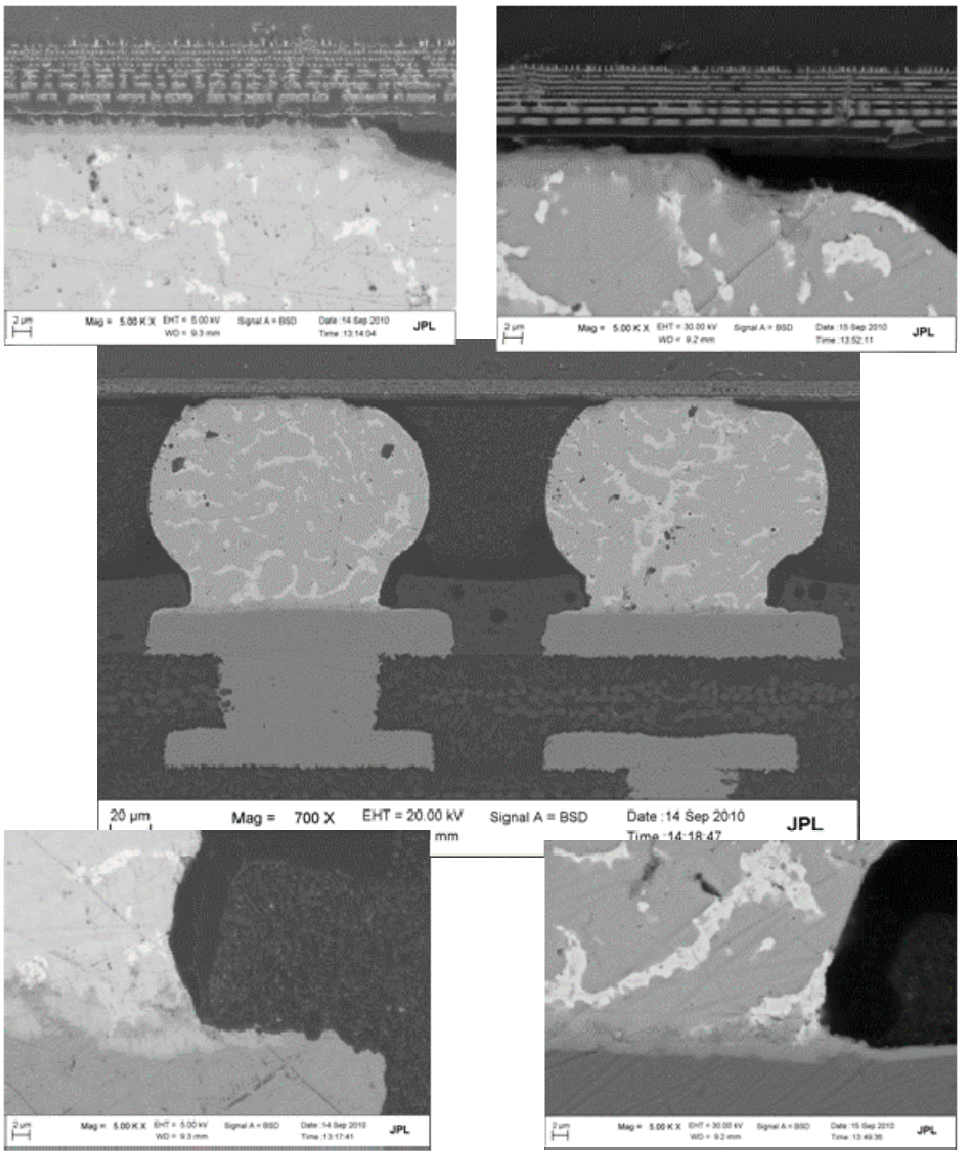

Figure 19. Cross-sectional photomicrographs of FCBGA1704 assembly after thermal cycling showing detailed metallurgical features of flip-chip solder balls at the die level.

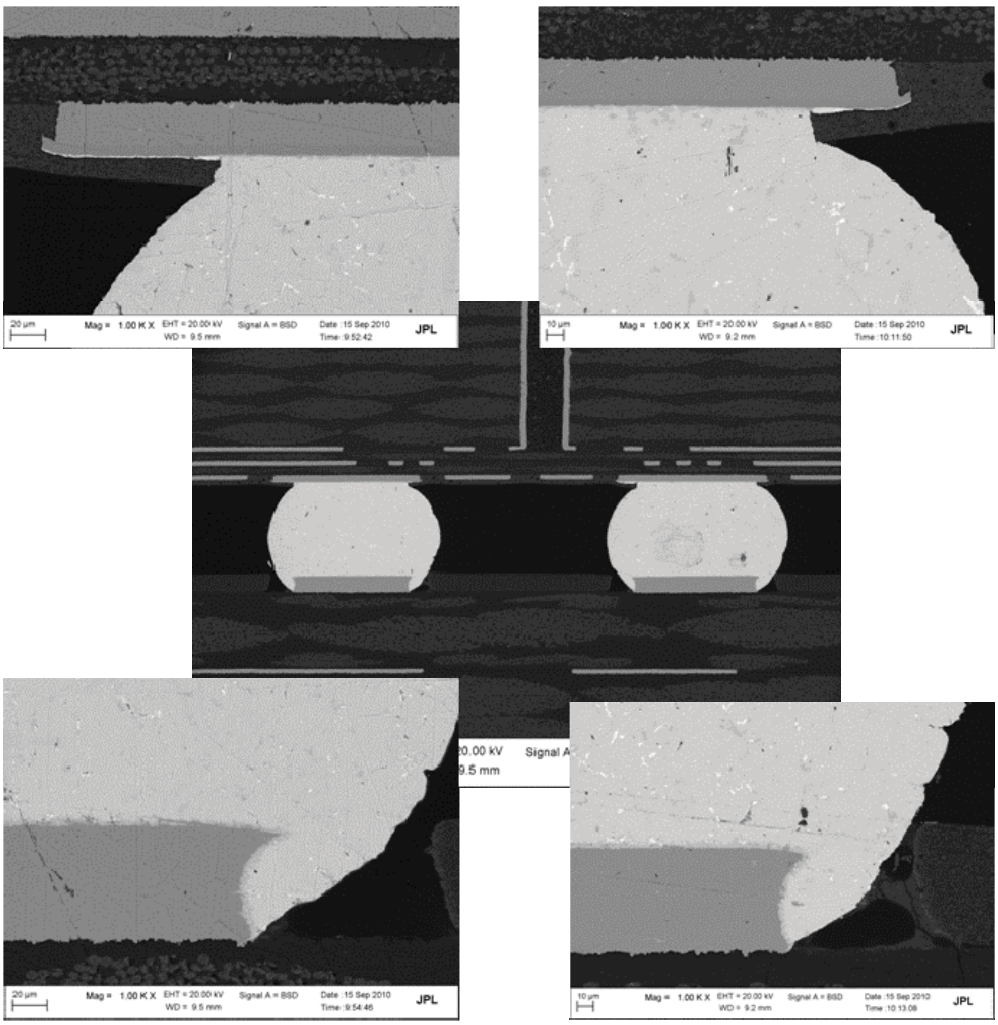

Figure 20. Cross-sectional photomicrographs of FCBGA1704 assembly after thermal cycling showing detailed metallurgical features of flip-chip solder balls at the package/board level.

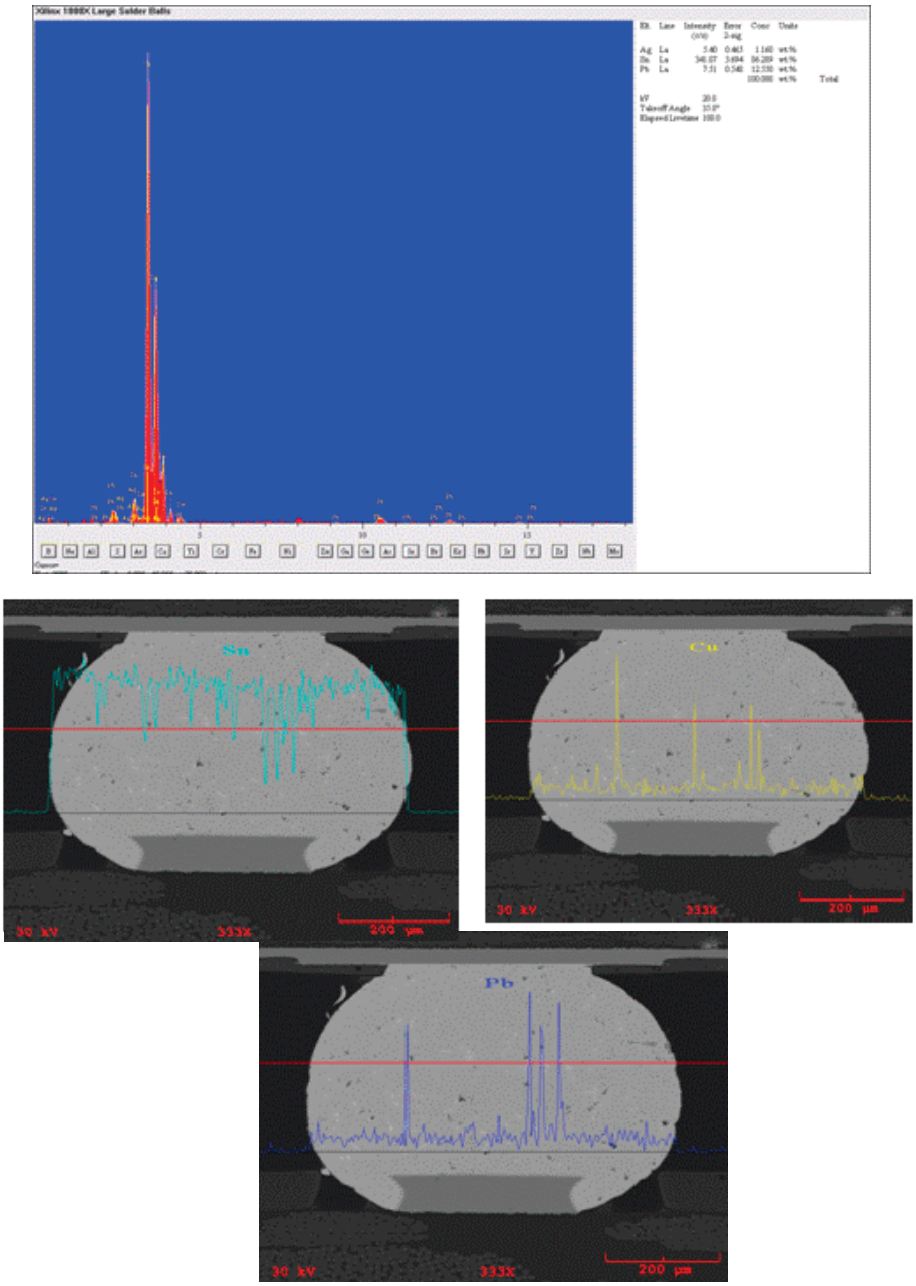

Figure 21. X-ray elemental analysis along the center line of FCBGA1704 for a solder ball at the package/board level.

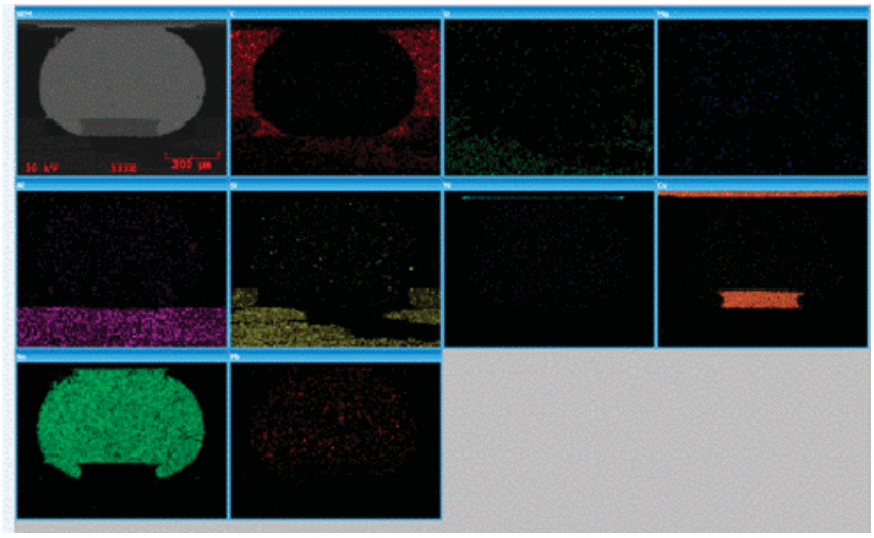

Figure 22. X-ray elemental mapping of FCBGA1704 for a solder ball at the package/board level.

6.6 Summary of Test Results by RIT University

A limited number of the test vehicles (TV3) with the FCBGA1704 package built at JPL as well as a large number of other test vehicles built at Rochester Institute of Technology (RIT) university were subjected to reliability evaluation by thermal cycles and mechanical dynamic loading. Recent reliability test results for those built by RIT Center for Electronics Manufacturing and Assembly (CEMA) were presented at the 60th IEEE Conference [11]. This comprehensive joint research aimed at making a comparison of assemblies built with tin-lead and various lead-free solder ball alloys for area array packages. PBGA676 was selected as the common package between the TV3 and those built by RIT. Package assembly reliability was compared for no-underfill, corner-underfill, and full-underfill. Assembly reliability was evaluated by subjecting the assemblies up to 60 mechanical drops in the as-assembled condition and after 200 or 500 thermal shock cycles.

To evaluate the solder joint reliability, assemblies were subjected to drop test prior to and after thermal shock (–55°C to 125°C) cycles. The ramp rate for the thermal shock cycle was 60°C/min and the dwell time was three minutes. The thermal shock equipment had to undergo defrosting after every 75 cycles for proper functioning. During the defrost period (approximately one hour) the assemblies are maintained at 125°C.

For the drop testing, assemblies were mounted in the horizontal orientation with components facing down. The board was held in place for the drop test, using the four corner tooling holes. This orientation is recommended since it provides the most severe board deflection as identified by JEDEC Standard No. 22-B111. The drop conditions were: (1) average peak load of 485 G, (2) time period of 3 ms, (3) stand-off-height of 2 inches, and (4) height of drop of 36 inches. After every drop the component solder joint integrity was evaluated using continuity measurement in the daisy chains. Generally test stopped after 30 drops but, in some cases when no failure occurred to 30 drops, the test was continued to 60 drops to possibly get failures for comparison.

Tables 4 and 5 summarize reliability test results for PBGA676 with SAC305 and SAC405 solder ball alloys, respectively, using SAC 305 solder paste for both cases. Reliability was much better for PBGA676 with full-underfill condition, when compared to those with corner-underfill or no-underfill conditions. For PBGA676 with SnAg solder ball alloy, however, noticeable improvement was achieved even for corner-underfill condition when compared to no underfill (see the Table 6). Full-underfill, SnAg assemblies survived up to 60 drops, including the ones subjected to 500 thermal shock cycles. Note that the location of this package type on PCB made them less susceptible to deflection and the strains due to repetitive drops.

Table 4. Number of drops to failure for PBGA676 I/O package with SAC 305 solder balls and solder paste.

PBGA676 Drops to Failure				
Solder paste (SAC305) – Solder ball (SAC305)				
Test Condition	PCB surface Finish	Without Underfill	Corner Underfill	Full Underfill
As Soldered	ENIG	3	5	43
	HASL	3	8	30
	ImAg	4	3	41
200 TS	ENIG	3	3	60-DNF
	HASL	5	2	33
	ImAg	2	2	38
500 TS	ENIG	2	4	60-DNF
	HASL	3	3	16
	ImAg	3	3	59

Table 5. Number of drops to failure for PBGA676 I/O package with SAC 405 solder balls and solder paste.

PBGA676 Drops to Failure				
Solder paste (SAC305) – Solder ball (SAC405)				
Test Condition	PCB surface Finish	Without Underfill	Corner Underfill	Full Underfill
As Soldered	ENIG	3	2	43
	HASL	2	8	47
	ImAg	1	3	60-DNF
200 TS	ENIG	2	2	60-DNF
	HASL	4	3	60-DNF
	ImAg	4	2	60-DNF
500 TS	ENIG	3	4	60-DNF
	HASL	3	5	60-DNF
	ImAg	5	4	60-DNF

Table 6. Number of drops to failure for PBGA676 I/O package with SnAg solder balls and solder paste.

PBGA676 Drops to Failure				
Solder paste (SAC305) – Solder ball (SnAg)				
Test Condition	PCB surface Finish	Without Underfill	Corner Underfill	Full Underfill
As Soldered	ENIG	12	DNF	60-DNF
	HASL	18	DNF	60-DNF
	ImAg	8	DNF	60-DNF
200 TS	ENIG	12	DNF	60-DNF
	HASL	13	DNF	60-DNF
	ImAg	7	17	60-DNF
500 TS	ENIG	*DNF	DNF	60-DNF
	HASL	13	25	60-DNF
	ImAg	22	18	50

Table 7 shows the number of drops to failure for a TV3 test vehicle (TV3-SN002) built at JPL. The failures for only 10 drops are listed even though the test vehicle was subjected to a total of 30 drops. The data were truncated because all packages, except one, failed under 10 drops. The highest drop numbers with no failure was for the PBGA676 package identified as E, located at the top left corner of the TV. This package survived 30 drops. The lowest drop number with failure detection after only one drop was for the large FCBGA1704 package identified as G, located at the center of the PCB; it possibly endured maximum deflection. Thermal shock cycle resistance of this package, however, was acceptable. The FCBGA, however, showed acceptable resistance thermal shocks with no failure to 500 cycles.

Table 7. Number of drops to failure for individual package assembly of TV3-SN002 including FCBGA1704.

Components		Pre-Drop	Drop 1	Drop 2	Drop 3	Drop 4	Drop 5	Drop 6	Drop 7	Drop 8	Drop 9	Drop 10
A	L1	0.080	0.086	0.086	0.081	0.080	0.080	0.073	0.080	0.076	0.080	0.086
	L2	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV
	R1	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV
	R2	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV
B	L1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	L2	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	R1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	R2	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
C	L1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	L2	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	R1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	R2	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
D	L1	1.442	1.445	1.449	1.561	DCF	DCF	DCF	DCF	DCF	DCF	DCF
	L2	1.758	1.764	1.766	1.862	DCF	DCF	DCF	DCF	DCF	DCF	DCF
	L3	0.313	0.320	0.315	0.302	0.314	0.303	0.318	0.305	0.321	0.300	0.312
	L4	0.324	0.323	0.316	0.313	0.315	0.304	0.321	0.305	0.322	0.304	0.315
	L5	0.754	0.764	0.756	0.75	0.753	0.744	0.761	0.748	0.762	0.742	0.755
	R1	0.836	0.835	0.839	0.831	0.831	0.821	0.843	0.826	0.863	0.823	0.836
	R2	1.159	1.164	1.168	1.244	DCF	DCF	DCF	DCF	DCF	DCF	DCF
	R3	1.163	1.168	1.173	1.294	DCF	DCF	DCF	DCF	DCF	DCF	DCF
	R4	1.355	1.360	1.363	1.491	DCF	DCF	DCF	DCF	DCF	DCF	DCF
E	L1	1.407	1.409	1.405	1.4	1.402	1.395	1.414	1.409	1.415	1.394	1.407
	L2	1.724	1.731	1.73	1.716	1.717	1.716	1.733	1.726	1.731	1.708	1.724
	L3	0.308	0.316	0.301	0.303	0.305	0.293	0.31	0.306	0.312	0.294	0.304
	L4	0.307	0.317	0.31	0.305	0.306	0.296	0.311	0.07	0.313	0.3	0.306
	L5	0.733	0.738	0.738	0.732	0.732	0.725	0.739	0.736	0.742	0.726	0.733
	R1	0.813	0.814	0.814	0.812	0.809	0.803	0.817	0.811	0.819	0.801	0.812
	R2	1.129	1.133	1.131	1.126	1.124	1.122	1.136	1.131	1.137	1.118	1.133
	R3	1.134	1.137	1.134	1.129	1.128	1.125	1.134	1.135	1.14	1.12	1.135
	R4	1.324	1.333	1.328	1.319	1.319	1.314	1.331	1.325	1.331	1.306	1.325
G	L1	6.005	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad
	L2	6.418	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad
	L3	7.477	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad
	R1	6.001	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad
	R2	6.382	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad
	R3	6.022	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad	CF-Pad
I	L1	0.781	0.785	0.786	0.787	0.791	0.802	14.62	5.998	5.86	DCF	DCF
	L2	0.731	0.735	0.735	0.736	0.74	0.742	22.659	6.094	6.411	DCF	DCF
	R1	0.122	0.126	0.124	0.122	0.123	0.114	0.131	0.13	0.138	0.146	0.2
	R2	0.171	0.175	0.173	0.173	0.175	0.168	21.422	4.335	11.144	DCF	DCF
J	L1	0.614	0.622	0.617	0.62	0.62	0.623	0.624	0.623	0.627	DCF	DCF
	L2	0.571	0.575	0.571	0.573	0.577	0.572	0.589	0.589	0.592	0.572	0.59
	R1	0.113	0.119	0.113	0.113	0.114	0.104	0.122	0.116	0.124	0.105	0.117
	R2	0.135	0.139	0.135	0.134	0.138	0.124	0.145	0.14	0.144	0.127	0.138
K	L1	0.764	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF
	L2	0.718	4.802	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF
	R1	0.122	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF
	R2	0.170	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF	DCF
L	L1	1.635	1.636	1.635	1.633	1.631	1.638	1.629	1.636	1.642	1.628	1.642
	L2	1.990	1.996	1.996	1.994	DCF	DCF	DCF	DCF	DCF	DCF	DCF
	L3	0.338	0.340	0.334	0.337	0.339	0.335	0.343	0.333	0.339	0.33	0.339
	L4	0.341	0.343	0.338	0.338	0.34	0.335	0.344	0.333	0.339	0.332	0.34
	L5	0.815	0.817	0.814	0.813	0.813	0.812	0.821	0.81	0.816	0.806	0.817
	R1	0.911	0.916	0.909	0.907	0.907	0.908	0.916	0.906	0.913	0.9	0.916
	R2	1.282	1.285	1.282	1.281	1.281	1.285	1.295	1.283	1.293	1.274	1.291
	R3	1.287	1.290	1.288	1.285	1.285	1.29	1.298	1.288	1.294	1.28	1.295
	R4	1.519	1.522	1.519	1.516	1.518	1.522	1.531	1.52	1.527	1.513	1.528
M	L1	1.791	1.795	1.794	1.787	1.788	1.797	1.886	DCF	DCF	DCF	DCF
	L2	2.170	2.169	2.172	2.162	2.167	2.174	2.187	DCF	DCF	DCF	DCF
	L3	0.365	0.369	0.365	0.365	0.365	0.359	0.372	0.361	0.368	0.359	0.365
	L4	0.368	0.377	0.361	0.36	0.368	0.363	0.374	0.361	0.368	0.36	0.367
	L5	0.886	0.890	0.887	0.883	0.884	0.884	0.894	0.883	0.89	0.878	0.881
	R1	0.990	0.996	0.99	0.998	0.987	0.988	1.001	0.984	0.997	0.982	0.995
	R2	1.393	1.397	1.393	1.39	1.39	1.393	1.405	DCF	DCF	DCF	DCF
	R3	1.399	1.401	1.399	1.395	1.395	1.399	1.412	DCF	DCF	DCF	DCF
	R4	1.658	1.658	1.66	1.653	1.656	1.661	1.672	DCF	DCF	DCF	DCF

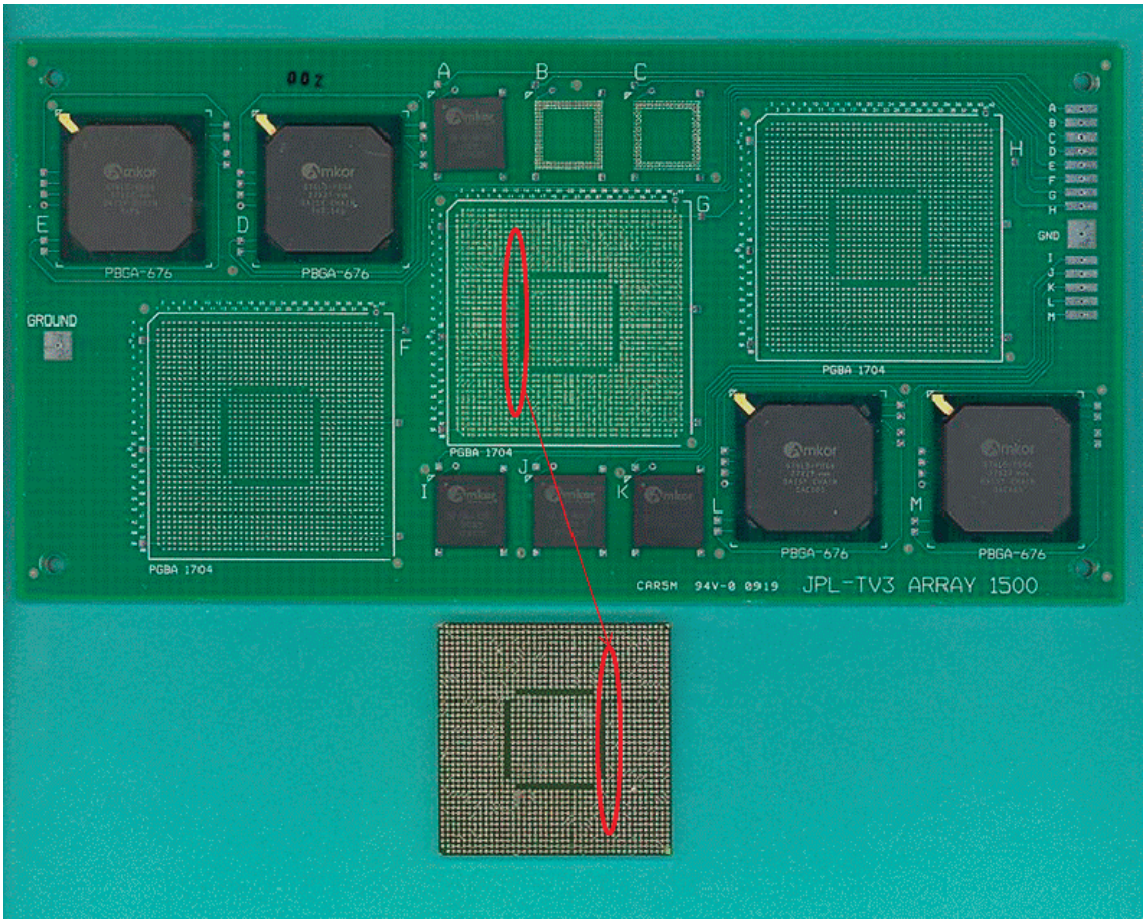

Figure 23. Photograph of the TV subjected to 30 drops showing that about 99% of failures occurred at the board level. Most solder balls remained on the package.

7. Conclusions

The conclusions, based on the results of thermal cycling with different profiles and drop tests using limited flip-chip ball grid array (FCBGA) 1704 input/output (I/O) and other package assemblies, are as follows:

- FCBGA1704 with 1.0-mm pitch had acceptable solder paste print quality whereas FPGA432 with 04-mm pitch generally had unacceptable conditions.
- FCBGA1704 showed high assembly yield even when a ministencil was used for paste print and/or a rework station was used for reflowing solder paste whereas FPGA432 showed poor assembly yield.
- The two-dimensional (2D) x-ray system used in this investigation revealed shorts and, in some cases, apparent opens for PBGA676 and FPBGA432. It did not reveal, however, a possible open for the only FCBGA1704, which showed daisy-chain open after assembly.
- FCBGA1704 and PBGA676 with 1.0-mm pitch with acceptable quality after assembly showed no daisy-chain resistance failures to 200 thermal cycles under the four different thermal cycle conditions (–55° to +100°C, –55° to +125°C, and –125°/+125°C, and thermal shock cycle in the range of –55° to +100°C). Results for FPBGA432 are not clear because of initial poor quality.
- FCBGA1704 showed minimum signs of damage after thermal cycling evaluated by cross-sectioning and SEM.
- FCBGA1704 with lead-free solder balls that assembled with tin-lead solder paste showed no apparent signs of segregation between the two solder alloys after thermal cycling evaluated by SEM and EDS mapping.
- The FCBGA1704 with 1.0-mm pitch located at the center of test vehicle, when subjected to drop loading of 485 g, failed after the first drop. This clearly shows sensitivity of large BGA packages to dynamic loading and high deflection deformation.
- PBGA676 with 1.0-mm pitch showed better resistance to drops, possibly because their smaller size and lighter weight make them less susceptible to failure compared to FCBGA1704. Another critical factor was that, because of their locations, these packages were exposed to less board deflection during drop testing since they were located away from the center of the board.
- The two-dimensional (2D) x-ray system used in this investigation did not reveal the level of solder damage or opens detected by daisy chain after thermal cycling.
- A summary of test data generated in collaboration with university and industry partners along with references to joint publications on these subjects were also presented.

8. NASA Application

This report covered qualification and verification steps and tools for flip-chip ball grid array (FCBGA) 1704 inputs/outputs (I/Os) and two other plastic BGA (PBGA) packages assembled onto printed circuit boards (PCBs). Prior to design, it is recommended to review numerous industry standards on this subject, including IPC 7095 and IPC 97xx (including 9701A), covering qualification approaches for thermal and mechanical characterizations. It is also recommended to review National Aeronautics and Space Administration (NASA) specifications, including NASA-STD-8739.3 (Soldered Electrical Connections) and NASA-STD-8739.2 (Workmanship Standards for Surface Mount Technology) and note applicable areas for quality, process controls, and solder. Applicable guideline documents for devices, as well as BGAs and CSPs published under the NASA Electronic Parts and Packaging (NEPP) Program (http://nepp.nasa.gov), should also be reviewed. Recommendations for NASA mission implementation are as follows:

- Ensure that all constraints on the use of plastic packages, including BGAs and CSPs, are well understood:
  - ✓ Use hermetic seal packages such as CQFPs and CCGA, if possible.
  - ✓ No pure tin finish is allowed. Use of lead-free alloys shall be approved for applications.
  - ✓ Use hot air solder leveling (HASL) surface finish for PWB and avoid immersion gold on Ni or other exotic finishes.
- Define the overall NASA mission environmental requirements, including radiation, mechanical, thermal, life cycle, mechanical shock, vibration, etc.
- Define appropriate potential package technology and types, including ceramic packages, high I/O flip-chip BGAs, low and high I/O PBGAs, low-pitch CSP and fine pitch BGAs, flip chip, leaded package, and MLF. Review build up, materials, solder geometry and alloys, heat distribution, etc., using package supplier data and application notes.
- Review application notes carefully for any design that will later exacerbate the condition, either during initial package burn-in thermal evaluation or subsequently during manufacturing: for example, die exposure to aggressive cleaning through venting hole or damage to FCBGAs underfill due to cleaning or long-time high temperature exposures.
- Determine if package properties are within the envelope of mission environmental requirements in order to avoid early overstress failures. Examples include radiation capability of die, temperature limits of package materials, including softening temperature (glass transition temperature, Tg), and junction temperature. Determine if special handling, bake out, assembly process, and tools are required.
- For life thermal cycle qualification, determine life cycle requirements for the mission. For the purpose of further narrowing package selection, consider the following four categories of NASA missions:

- ✓ A: Benign thermal cycle exposure with short mission duration (e.g., Space Shuttle missions)
- ✓ B: Benign thermal cycles with long mission duration (International Space Station, Hubble Space Telescope, Mars Reconnaissance Orbiter [MRO], GRAIL, etc.)
- ✓ C: Extreme thermal cycles with short mission duration (Mars Exploration Rover [MER], etc.)
- ✓ D: Extreme temperature cycle exposure with long mission duration (Web Space Telescope [JWST], Mars Science Laboratory [MSL], etc.)

- If details on life cycle requirements are not available, then use the following rules of thumb to estimate the number of accelerated thermal cycles for NASA missions:
  - ✓ For A and B missions, thermal life cycle requirements are estimated to vary from 100 to 500 accelerated cycles in the range of −55°C to 100°C (NASA cycle).
  - ✓ For C and D missions, estimate the flight allowable temperature ranges and multiply mission cycles by 3. If mission cycle duration is short, add an additional 20 NASA cycles to include the cycle consumption for ground testing.
- Review heritage and package supplier's data for package- and second-level solder joint reliability. Use the following generic guidelines for meeting the requirements.
  - ✓ No flight heritage exists for high I/O flip-chip BGA, high I/O PBGA, and low-pitch CSP packages even though contract manufacturers may have already implemented use of lower I/O PBGAs in their electronic systems. Generally, these categories of packages have been shown to have adequate thermal cycle resistance.
- Flip-chip BGAs with 1500–2500 I/Os have thermal cycle and dynamic mechanical loading resistance limitation and should be carefully evaluated before intended use.
- High I/O PBGAs (500–100 I/Os) with internal wire bond attachments meet most non-extreme NASA environmental requirements (A and B conditions). Use of PBGA requires additional part/die qualification and verification for application.
  - ✓ Flip-chip die BGA packages (500–1000 I/Os) may have lower thermal and mechanical resistance, but that may be adequate for A mission and potentially for B missions.
- Use of CSP and flip-chip die direct attachment should be restricted and, only after careful review of vendor data and acceptability, be qualified for specific applications.
- Use a daisy-chain package as the test article for accelerated thermal cycle tests as specified in IPC 9701A. Daisy-chain packages are generally built using similar materials and layup as the functional package with the exception of using a dummy die with even/odd pad connections. Die size affects solder joint reliability and, therefore, should be the same size or larger than the flight-like package.

- Design double-sided assembly if it mimics flight configuration. However, note that double-sided, mirror-image assemblies show major reduction in solder joint reliability.
- Optimize reflow thermal profile, especially for a mixed technology assembly. Remember that process optimization and process control are key parameters that control solder attachment integrity for area array packages, not optical/visual inspection, as commonly used for most other electronic packages at NASA. Refer to NASA standards for use of flux, solder paste quality test, and cleanliness requirements.
- Perform real-time x-ray and optical inspection, if possible. Use of an x-ray machine with laminography capability is recommended.
  - ✓ The 2D x-ray system used in this investigation did not reveal the level of solder damage due to thermal cycling.
- Prior to x-sectioning, SEM evaluation of the outer rows of package assembly should be performed to reveal damage not detected by optical microscopy. X-section should be performed to reveal internal damage and crack formation.

In summary, it was shown that flip-chip BGA with 1704 I/Os, fully populated balls, and 1.0-mm pitch has moderate resistance to thermal cycling and low resistance to dynamic loading when using conventional tin-lead eutectic solder paste for their assembly. The wire-bonded PBGA with 767 I/Os, fully populated balls, and 1.0-mm pitch have acceptable thermal cycle reliability when assembled with tin-lead solder. Fine-pitch BGAs with 0.4-mm pitch showed poor assembly yield and therefore need further optimization before providing reliability ranking

The key drawbacks of FCBGA, PBGA, and fine-pitch array packages remain the same, i.e., inspection capability for interconnection integrity (cracks) and individual solder ball re-workability. In addition, most array packages are commercial-off-the-shelf (COTS) packages; they are required to be subjected to additional stringent screening with added cost at the package level prior to their acceptance for NASA applications.

9. Acronyms and Abbreviations

BGA	ball grid array
CBGA	ceramic ball grid array
CCGA	ceramic column grid array
CEMA	Center for Electronics Manufacturing and Assembly
CGA	column grid array
COTS	commercial-off-the-shelf
CPMT	component, packaging and manufacturing technology
CSP	chip scale (size) package
CTF	cycles to failure
Cu	copper
DOE	design of experiment
EDX/EDS	energy dispersive x-ray
ENIG	electroless nickel immersion gold
FCBGA	flip-chip ball grid array
FPBGA	fine-pitch BGA, also known as chip scale package (CSP)
FC/DCA	flip-chip direct chip attach
HASL	hot-air solder leveling
HCI	hot carrier induced
IC	integrated circuit
IEEE	Institute of Electrical and Electronics Engineers
ImAg	immersion silver
IMAPS	International Microelectronics and Packaging Society
I/O	input/output
iNEMI	International Electronics Manufacturing Initiative
IPC	association connecting electronics industries
JPL	Jet Propulsion Laboratory
JWST	James Web Space Telescope
MER	Mars Exploration Rovers
MIP	mandatory inspection point
MLF	microlead frame
MRO	Mars Reconnaissance Orbiter
MSL	Mars Science Laboratory
NASA	National Aeronautics and Space Administration
NBTI	negative biased temperature instability
NEPP	NASA Electronic Parts and Packaging
Ni	nickel
NSMD	non solder mask defined
PBGA	plastic ball grid array

PCB	printed circuit board
PWB	printed wiring board
QA	quality assurance
QFP	quad flat pack
RIT	Rochester Institute of Technology
SEM	scanning electron microscopy
SET	single event transient
SEU	single event upset
SMC	surface mount components
SMD	solder mask defined
SMT	surface mount
SMTA	Surface Mount Technology Association
TDDB	time-dependant dielectric breakdown
Tg	glass transition temperature
TV	test vehicle

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11. References

[1] International Electronics Manufacturing Initiative (iNEMI), Research Priorities, 2005, pp. 11, www.inemi.org.

[2] Fjelstad, J., Ghaffarian, R., and Kim, Y.G., *Chip Scale Packaging for Modern Electronics* (Electrochemical Publications, 2002).

[3] Ghaffarian, R., "Chip Scale Package Assembly Reliability," Chapter 23 in *Area Array Interconnect Book*, eds. K. Puttlitz, and P. Totta (Kluwer Academic Publishers, 2002).

[4] Ghaffarian, R., "BGA Assembly Reliability," Chapter 20 in *Area Array Packaging Handbook*, ed. K. Gilleo (McGraw-Hill, 2004).

[5] Ghaffarian, R., "Characterization and Failure Analyses of Lead-Free Solder Defects," Chapter 10 in *Lead-Free Solder Interconnect Reliability*, ed. D. Shangguan (ASM International, 2005).

[6] Ghaffarian, R., "Area Array Technology for High Reliability Applications," Chapter 16 in *Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging*, ed. E. Suhir (Springer, 2006).

[7] Ghaffarian, R., "Reliability of PWB Microvia for High Density Package Assembly," International Journal of Materials and Structural Integrity, 2008, Vol. 2, No. 1–2, pp. 47–63.

[8] Ghaffarian, R., "Thermal Cycle Reliability and Failure Mechanisms of CCGA and PBGA Assemblies with and without Corner Staking," *IEEE Transactions on Components and Packaging Technologies*, June 2008, Vol. 31, Issue 2.

[9] Ghaffarian, S. Bagheri, H. McCormick, and I. Sterian, "Reliability of Lead-Free and Tin-Lead Solders for PBGA Assemblies," IMAPs RF Packaging Workshop, San Diego, 16–18 September 2008.

[10] Bankeem, V.C., Ramkumar, S.M., Ghaffarian, R., " Thermal Shock and Drop Test Performance of Lead-Free Assemblies with No-Underfill, Corner-Underfill, and Full-Underfill," The Proceedings of 60th IEEE Electronic Components and Technology Conference, Las Vegas, NV, June 1–4, 2010.

[11] Ghaffarian, R., "Area Array Package Trends and Assembly Reliability Failures for Tin-lead and Lead-free Solders," Components for Military and Space Electronics Conference (CMSE), Los Angeles, CA, Feb. 11. 2010.

[12] Mawer, A. and Luquette, L., "Interconnect Reliability of Ball Grid Array and Direct Chip Attach," *IRPS 1997 Tutorial*, 1997.

[13] http://www.amkor.com

[14] http://www.altera.com

[15] http://www.xilinx.com

[16] Shiah, A.C., and Zhou, X., "A Low Cost Reliability Assessment for Double-Sided Mirror-Imaged Flip Chip BGA Assemblies," *The Proceedings of Pan Pacific Conference*, Surface Mount Technology Association, 2002.

[17] Evans, J.W, Evans, J.Y., Ghaffarian, R., Mawer, A., Lee, K., and Shin, C., "Monte Carlo Simulation of BGA Failure Distributions for Virtual Qualification," *ASME*, Hawaii, 1991.

[18] IPC 9701, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments," IPC, Association Connecting Electronics Industries, 2002.

[19] Ghaffarian, R., "CSP Reliability for Single- and Double-Sided Assemblies," *Chip Scale Rev.*, 1999, Vol. 3, pp. 34–39.

[20] Newman, K., Freda, M., Ito, H., Yama, N., and Nakanishi, E., "Enhancements in 175FPBGA Board-Level Solder Joint Reliability through Package Constructions," *The Proceedings of the 6th Pan Pacific Microelectronics Symposium*, Kauai, HI, January 2001.

[21] Chaparala, S., et al., "Experimental and Numerical Investigation of the Reliability of Double-Sided Area Array Assemblies," *Journal of Electronics Packaging*, pp. 441–448, Vol. 128, December 2006.